

# Flessey PR2250



communication receiver

PART 2

## 10. MODULE 9A : SYNTHESISER

### 10.1 Introduction

Module 9A contains two phase-lock loop controlled oscillator circuits. One produces the fixed-frequency (63.6 MHz) 2nd local oscillator output, while the other produces the variable-frequency (65 to 95 MHz) 1st local oscillator output; this output can be varied in steps of 10 Hz.

### 10.2 Basic Principles

The basic phase-lock loop circuit employed is of the form shown in figure (a). The VFO output frequency is X times the reference frequency, where X is the division ratio of the loop divider circuit. If this division ratio is variable, the output frequency is also variable. The output frequency variation step-size is equal to the reference frequency applied to the comparator and this limits the minimum step-size. If, for example a 10 Hz reference frequency were employed then the output frequency could be varied in 10 Hz steps. However, the time taken for the loop to 'lock' increases as the reference frequency decreases, so there is a limit to the fineness of the minimum output step from the circuit shown in Figure (a). A divider is frequently inserted in the REF INPUT line to produce a suitable reference input frequency to the comparator.

10.2.1 Consider the circuit shown in Figure (b), wherein a mixer and a variable divider precede the circuit of Figure (a). The upper side-band output from the mixer is applied to the 'reference' input of the comparator. In Figure (b), let reference 2 be of variable frequency. Also, let both variable dividers at all times produce identical division ratios.

10.2.2 If both dividers in Figure (b) have a division ratio of X, then the final output frequency ( $f_o$ ) is X times the USB filter output frequency. The USB filter output frequency is:-

$$\text{REF 1} + \frac{\text{REF 2}}{X}$$

Therefore, the final output frequency  $f_o$  is

$$X(\text{REF } 1 + \frac{\text{REF } 2}{X})$$

or

$$X \cdot \text{REF } 1 + \text{REF } 2$$

and can be varied in two ways. Either term  $X$  (the divider ratio) or  $\text{REF } 2$  frequency can be varied to change the value of  $f_o$ .

This action is illustrated as follows:-

(i)  $\text{REF } 1 = 1 \text{ MHz}; \text{REF } 2 = 1.1 \text{ MHz}; X = 50; f_o = 50$   
 $(1 + \frac{1.1}{50}) = \underline{51.1 \text{ MHz}}$

(ii)  $\text{REF } 1 = 1 \text{ MHz}; \text{REF } 2 = 1.2 \text{ MHz}; X = 50; f_o = 50$   
 $(1 + \frac{1.2}{50}) = \underline{51.2 \text{ MHz}}$

(iii)  $\text{REF } 1 = 1 \text{ MHz}; \text{REF } 2 = 1.1 \text{ MHz}; X = 76; f_o = 76$   
 $(1 + \frac{1.1}{76}) = \underline{77.1 \text{ MHz}}$

ie  $f_o = X + \text{REF } 2$  where  $\text{REF } 1 = 1 \text{ MHz}$

10.2.3 If the circuit shown in Figure (b) is further modified by the inclusion of a divide-by-ten circuit between the USB filter output and the comparator input, then the output frequency is given by  $f_o = 0.1 (X + \text{REF } 2)$  where  $\text{REF } 1 = 1 \text{ MHz}$ . This arrangement can be used in a cascade loop as shown in Figure (c). The first stage is as shown in Figure (a); the second and third are as shown in Figure (b) with the divide-by-ten modification, and the fourth stage is as shown in Figure (b).

10.2.4 If terms  $W$ ,  $X$ ,  $Y$  and  $Z$  of Figure (c) are given values of  $W = 40$ ,  $X = 50$ ,  $Y = 60$  and  $Z = 70$ , then the frequencies at points A, B, C, and D in Figure (c) are as follows:-

$$\begin{aligned}
A &= (W \times \text{REF } 1) = 40 \times 1 = 40 \text{ MHz} \\
B &= 0.1(X+A) = 0.1(50+40) = 9 \text{ MHz} \\
C &= 0.1(Y+B) = 0.1(60+9) = 6.9 \text{ MHz} \\
D &= (Z+C) = (70+6.9) = 76.9 \text{ MHz}
\end{aligned}$$

10.2.5 Table 1 shows the effect of varying terms W, X, Y and Z separately. By this method, four division ratio controls (one for each stage) can be calibrated in terms of digits of the output frequency  $f_o$ . These controls can be further combined by external circuits into one single rotary knob.

TABLE 1 : VARIATIONS OF DIVIDER TERMS

| Divider Term |           |           |           | Varied by  | Varied by  | Varied by | Varied by    |
|--------------|-----------|-----------|-----------|------------|------------|-----------|--------------|
| W            | X         | Y         | Z         | Term Z     | Term Y     | Term X    | Term W       |
| 40           | 50        | 60        | 70        | 7 6        | . 9        | 0         | 0 MHz        |
| 40           | 50        | 60        | <u>80</u> | <u>8</u> 6 | . 9        | 0         | 0 MHz        |
| 40           | 50        | 60        | <u>71</u> | 7 <u>7</u> | . 9        | 0         | 0 MHz        |
| 40           | 50        | <u>60</u> | 70        | 7 7        | . <u>0</u> | 0         | 0 MHz        |
| 40           | <u>51</u> | 60        | 70        | 7 6        | . 9        | <u>1</u>  | 0 MHz        |
| 40.5         | 50        | 60        | 70        | 7 6        | . 9        | 0         | <u>5</u> MHz |

10.2.6 The range of variation of term Z is decided by the desired frequency range. The variations of terms Y and X are both over a range of ten. In the example given, the variation of term W is over a range of one in steps of 0.1 or less: in a practical circuit, term W is a division ratio of hundreds and therefore would vary over a larger range. The smallest step by which output frequency can be varied, so producing a circuit (Figure (c)) in which fine variations of frequency can be made, without incurring the penalty of long 'lock' time.

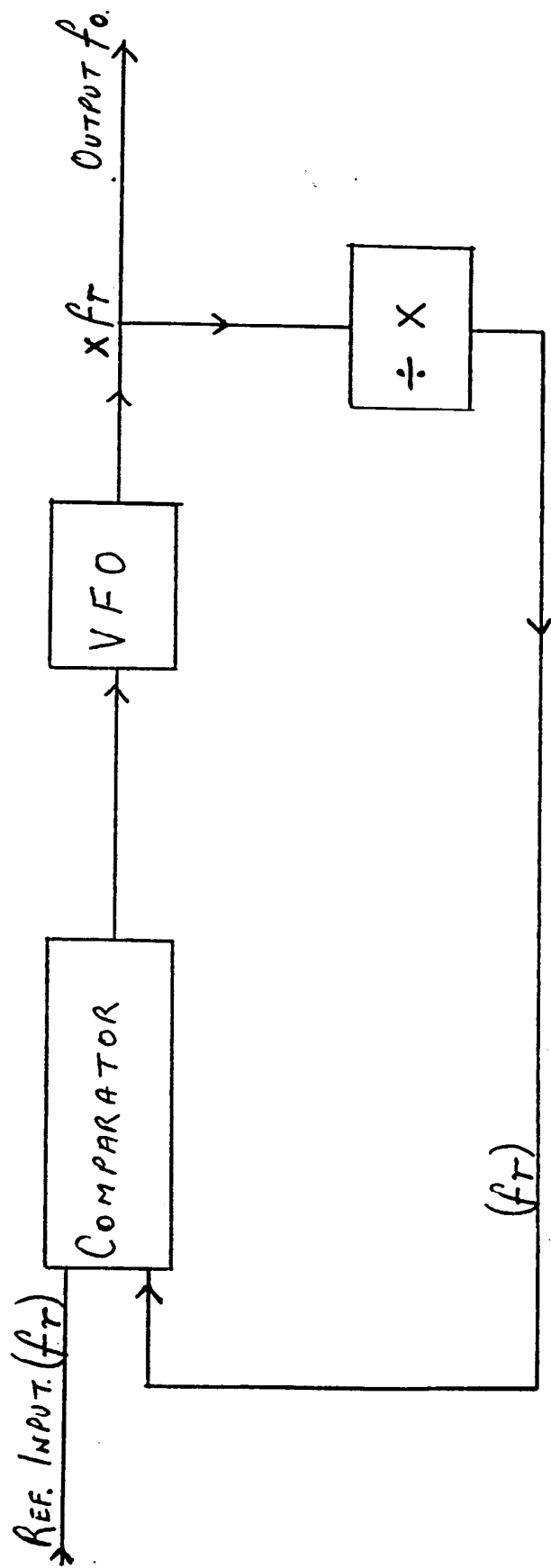


FIG. (a) BASIC PHASE-LOCK LOOP.

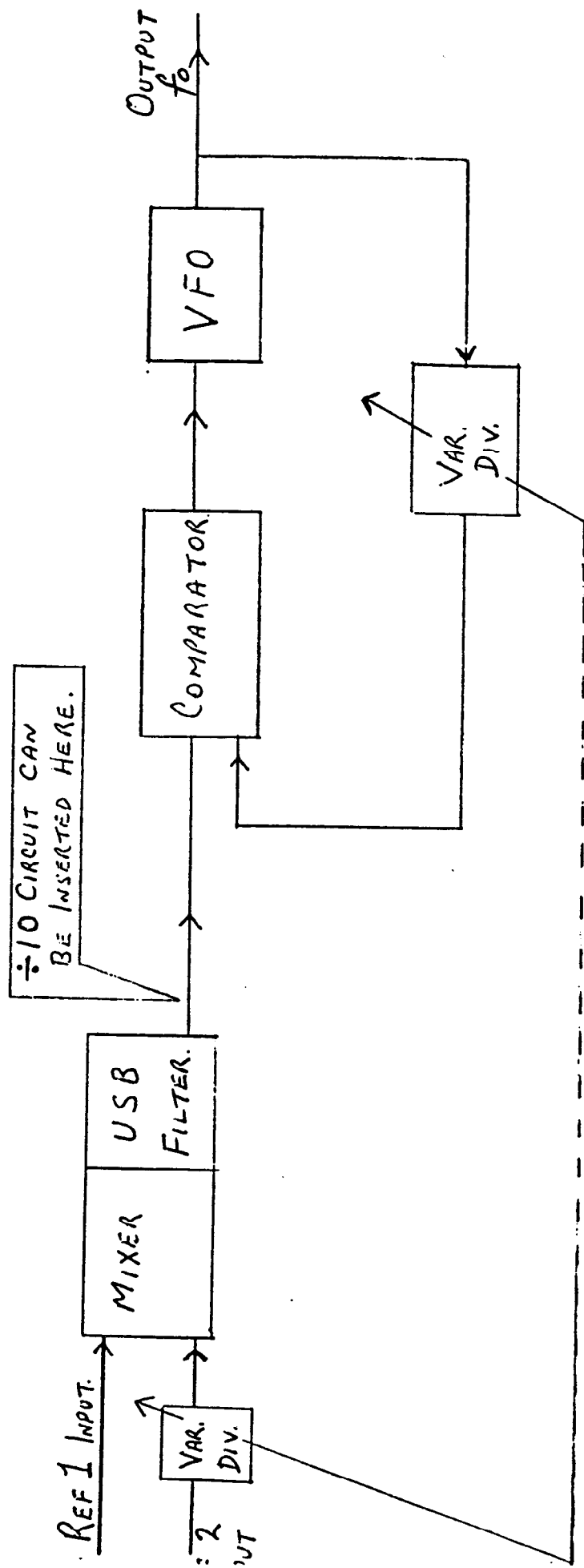


FIG (b) DEVELOPMENT OF FIG (a) CIRCUIT.

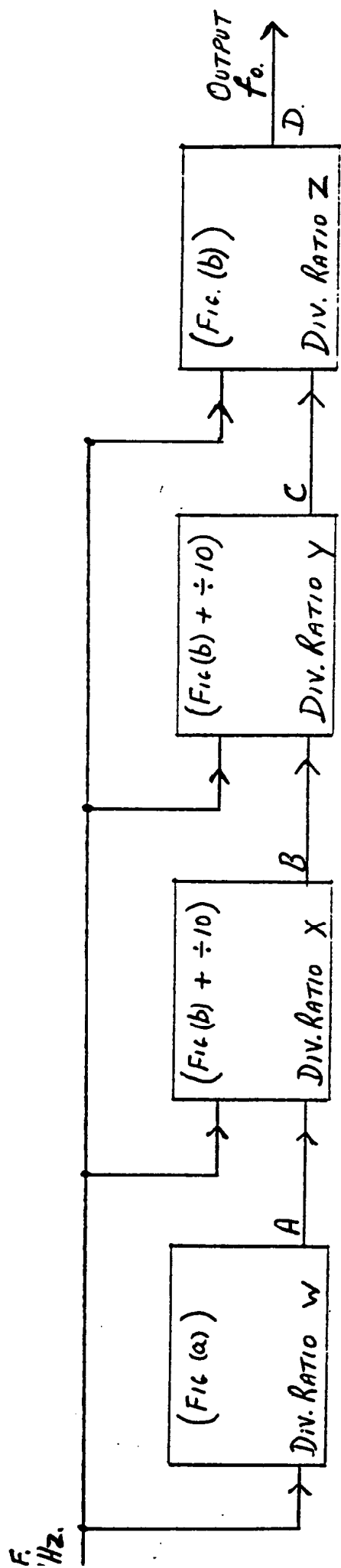
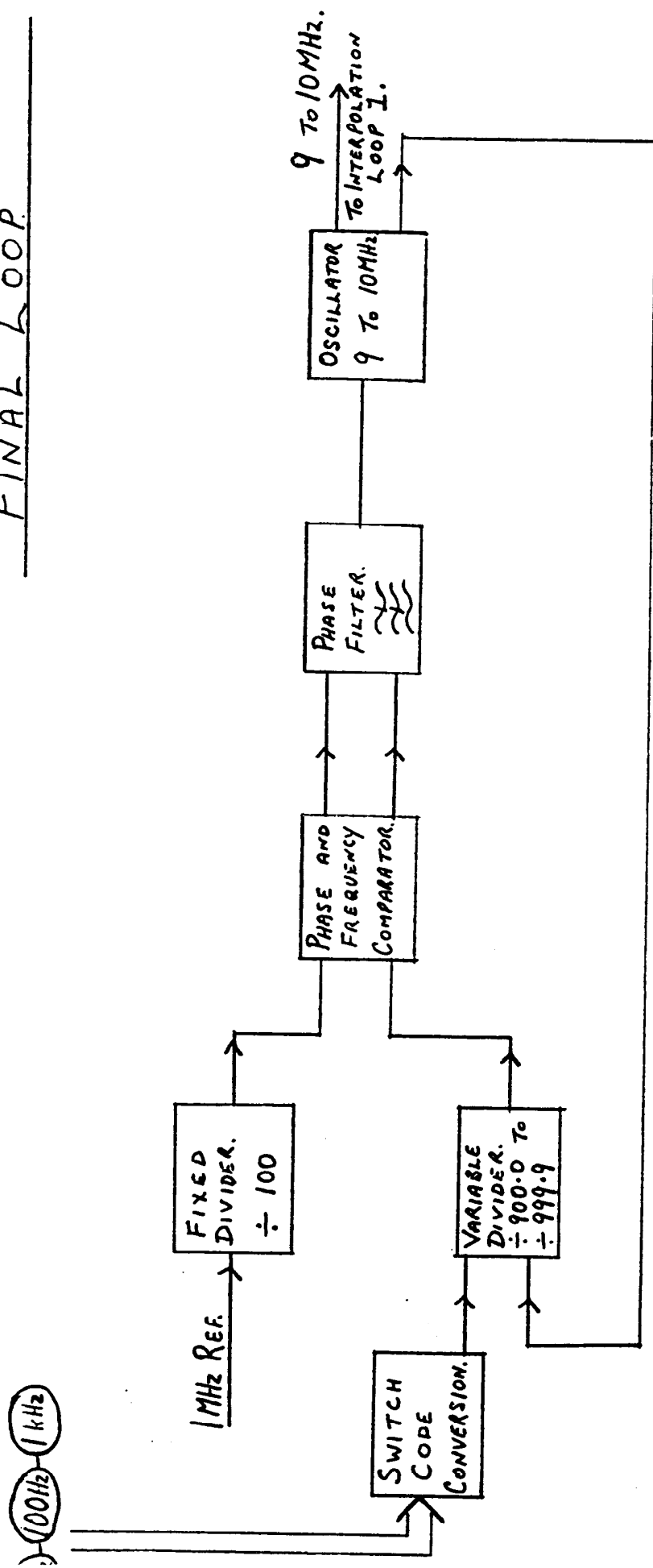


FIG. (c) FOUR - TERM CASCADE PHASE - LOCK LOOP.

# FINAL LOOP



MODULE 9A: SYNTHESISER.

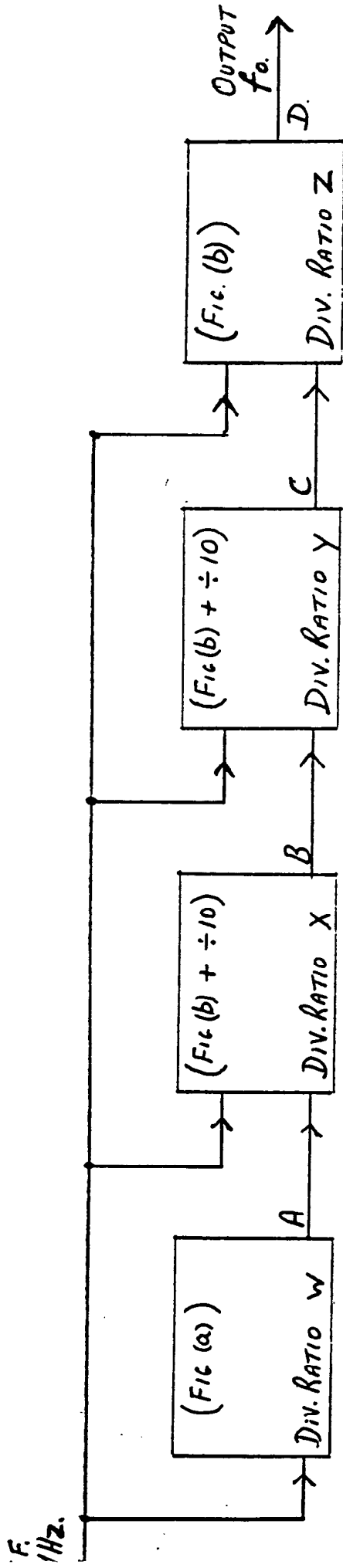


Fig. (c) Four - Term Cascade Phase - Lock Loop.

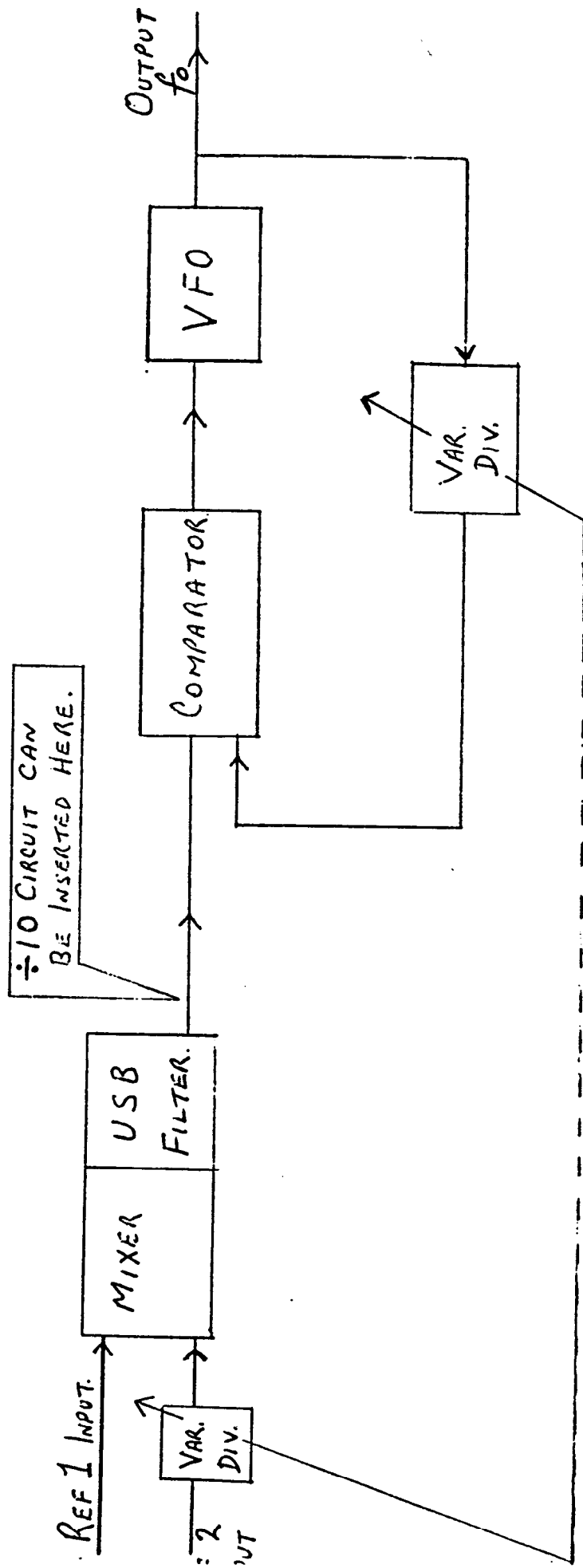


FIG (b) DEVELOPMENT OF FIG (a) CIRCUIT.

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|--------------|-----------|-----------|-----------|------------|------------|-----------|--------------|
| W            | X         | Y         | Z         | Term Z     | Term Y     | Term X    | Term W       |
| 40           | 50        | 60        | 70        | 7 6        | . 9        | 0         | 0 MHz        |
| 40           | 50        | 60        | <u>80</u> | <u>8</u> 6 | . 9        | 0         | 0 MHz        |
| 40           | 50        | 60        | <u>71</u> | 7 <u>7</u> | . 9        | 0         | 0 MHz        |
| 40           | 50        | <u>60</u> | 70        | 7 7        | . <u>0</u> | 0         | 0 MHz        |
| 40           | <u>51</u> | 60        | 70        | 7 6        | . 9        | <u>1</u>  | 0 MHz        |
| 40.5         | 50        | 60        | 70        | 7 6        | . 9        | 0         | <u>5</u> MHz |

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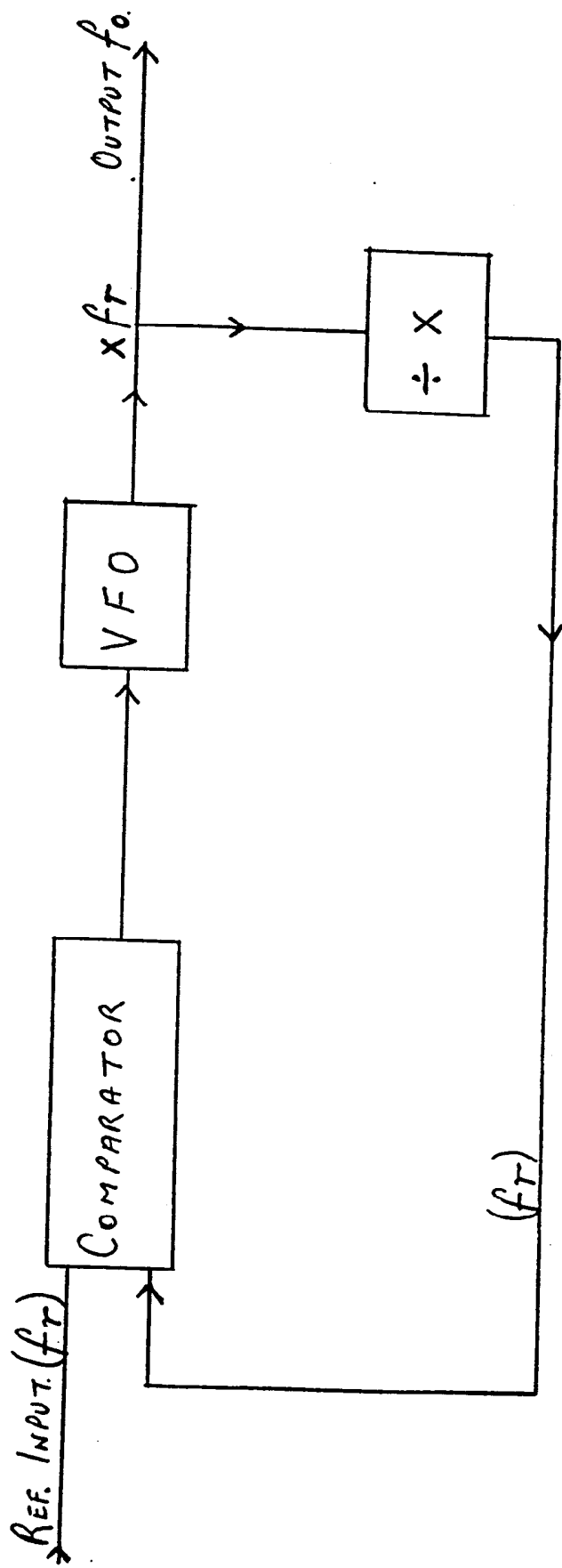


FIG. (a) BASIC PHASE-LOCK LOOP.

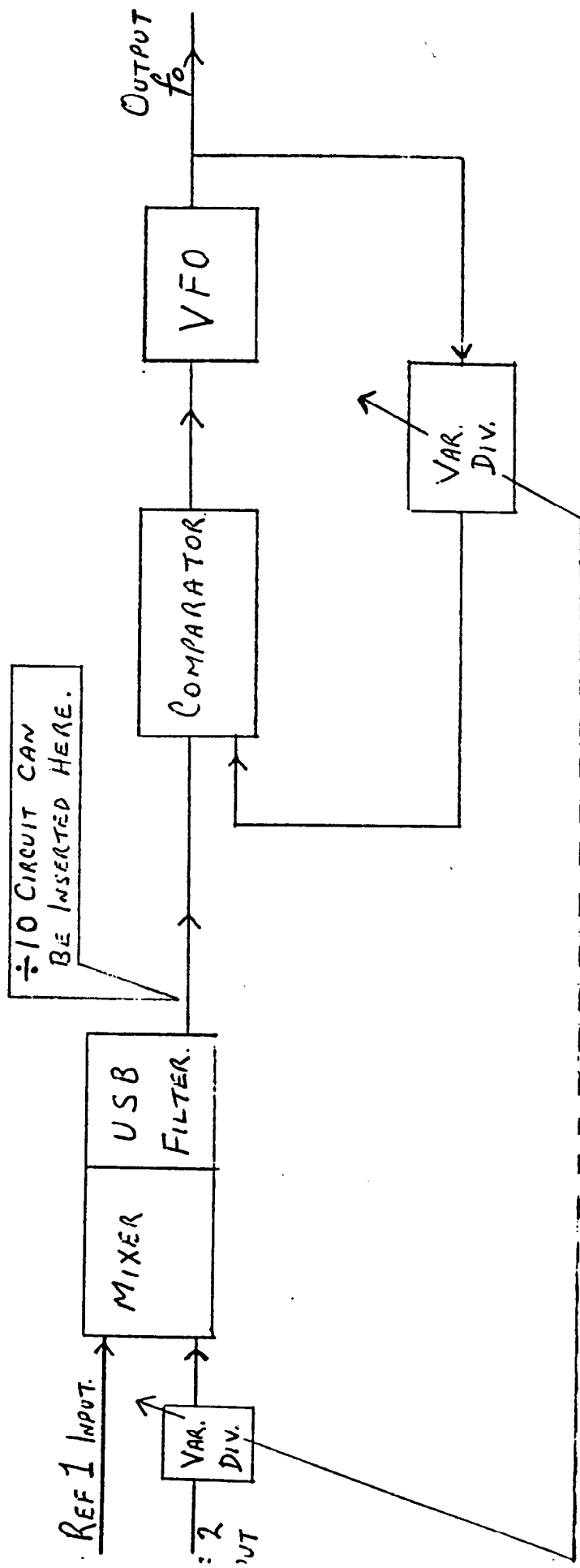


FIG (b) DEVELOPMENT OF FIG (a) CIRCUIT.

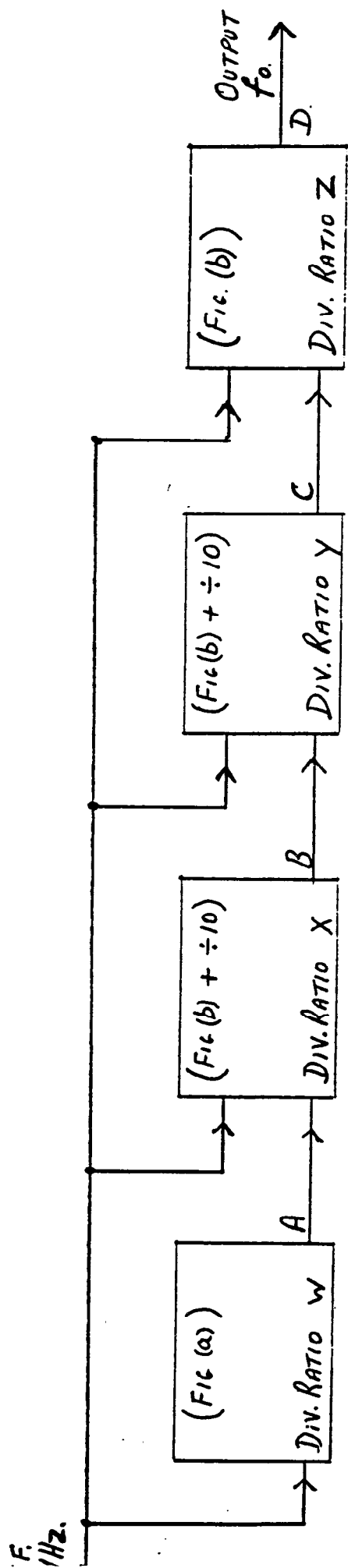
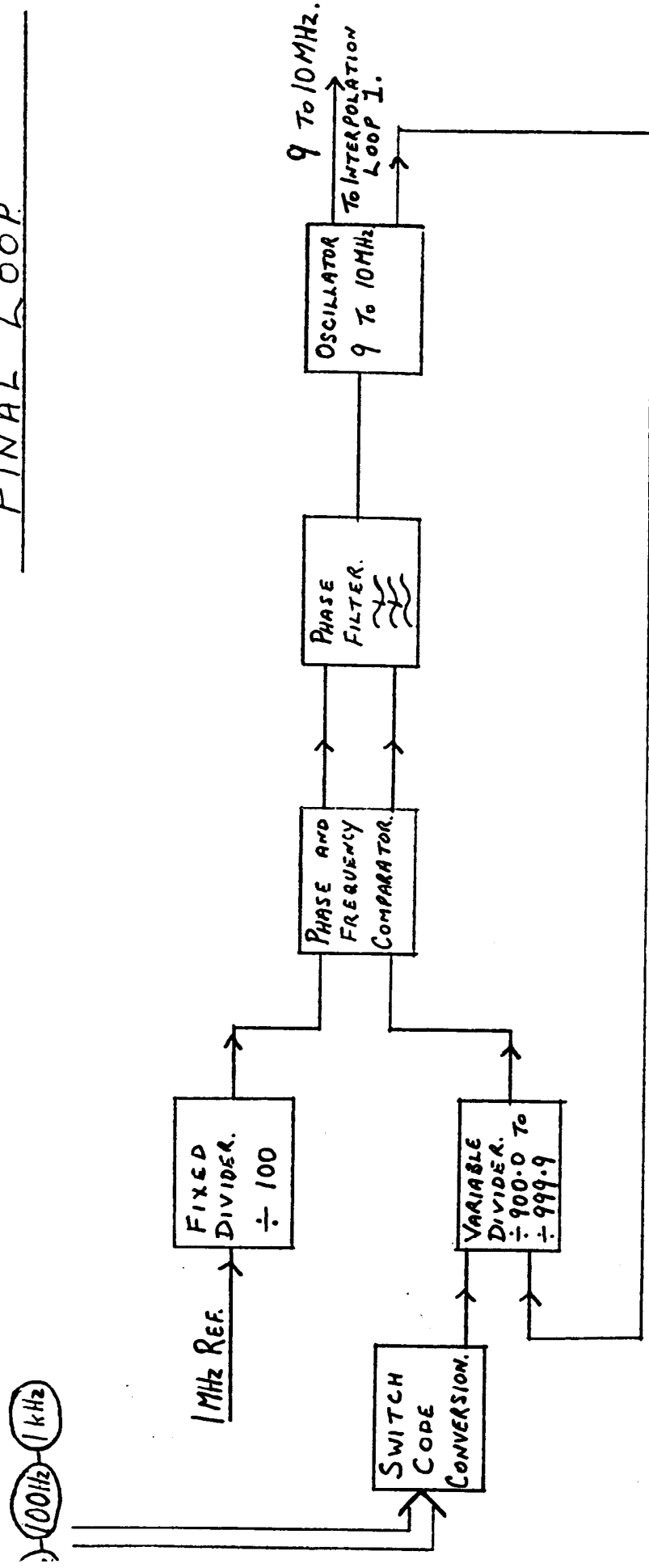


FIG. (c) FOUR - TERM CASCADE PHASE - LOCK LOOP.

# FINAL LOOP



MODULE 9A: SYNTHESISER.

### 10.3 Functional Description

#### 10.3.1 1st Local Oscillator

10.3.1.1 The 1st local oscillator circuit is composed of four sections, with each section controlled by one of the divider terms W, X, Y, and Z. The term values are:-

W : 900 to 999.9 (FINAL LOOP)

X : 81 to 90 (INTERPOLATION LOOP 1)

Y : 81 to 90 (INTERPOLATION LOOP 2)

Z : 56 to 85 (OUTPUT LOOP)

Variations of term values for given final output frequency shifts are as shown in Table 2.

TABLE 2 : VARIATIONS OF TERM VALUES

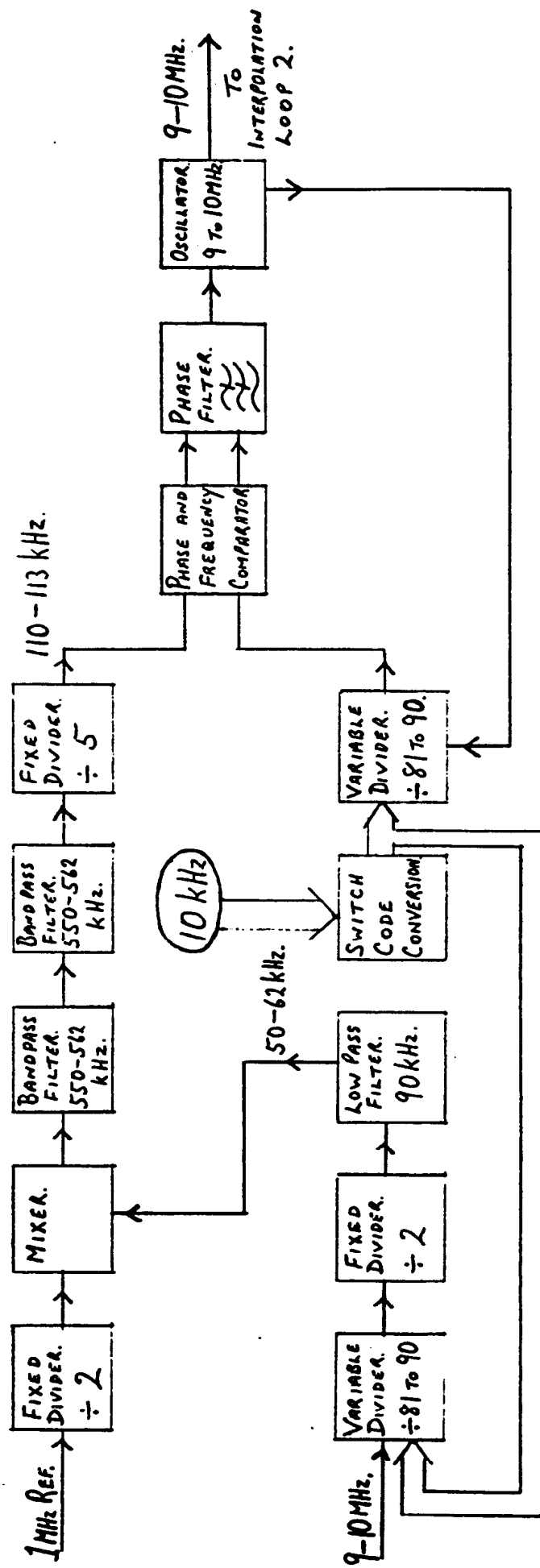
|     | 10 Hz | 100 Hz | 1 kHz | 10 kHz | 100 kHz | 1 MHz | 10 MHz |
|-----|-------|--------|-------|--------|---------|-------|--------|
| W : | 0.1   | 1      | 10    | -      | -       | -     | -      |
| X : | -     | -      | -     | 1      | -       | -     | -      |
| Y : | -     | -      | -     | -      | 1       | -     | -      |
| Z : | -     | -      | -     | -      | -       | 1     | 10     |

The first stage consists of the 'FINAL LOOP' circuit and is of the form shown in Figure (a). The 1 MHz REF input is divided down to 10 kHz : this, in conjunction with a term W division ratio variable between 900 and 999.9 produces a FINAL LOOP output frequency between 9 and 10 MHz which can be varied in steps of 10 Hz, 100 Hz or 1 kHz.

10.3.1.2 The output from the final loop is applied to the second stage, known as INTERPOLATION LOOP 1: The circuit is of the form shown in Figure (b) with the addition of a divide-by-ten circuit as previously described. Term X value is variable between 81 and 90: this, in conjunction with a 9 to 10 MHz input from the FINAL LOOP produces an output frequency between 9 and 10 MHz. A variation of one in term X produces an interpolation loop 1 output frequency variation of 10 kHz. The Interpolation loop 1 output frequency, therefore, is between 9 and 10 MHz and can be varied in steps of 10 kHz, 1 kHz, 100 Hz and 10 Hz (equivalent to output B in Figure (c)).

10.3.1.3 The output from the interpolation loop 1 is applied to the third stage, known as interpolation loop 2; this is identical with interpolation loop 1 and is housed on three similar printed circuit panels. A variation of one in term Y produces an interpolation loop 2 output frequency variation of 100 kHz. The output frequency is between 9 and 10 MHz and can be varied in steps of 100 kHz, 10 kHz, 1 kHz, 100 Hz and 10 Hz (equivalent to output C in Figure (c)).

## INTERPOLATION LOOP 1.



# Module 9A: Synthesiser.

10.3.1.4 The output from interpolation loop 2 is applied to the fourth stage known as the OUTPUT LOOP: the circuit is of the form shown in Figure (b), and no divide-by-ten action occurs. Although a divide-by-ten function exists on the reference input to the comparator, this is nullified by a divide-by-ten circuit placed on the variable divider line. The action therefore becomes the mathematical addition of term Z (MHz) to the output from interpolation loop 2 (MHz). A variation of one in term Z produces a 1 MHz output frequency step. The OUTPUT LOOP output frequency, therefore is between 65 and 95 MHz and can be varied in steps of 10 MHz, 1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz and 10 Hz.

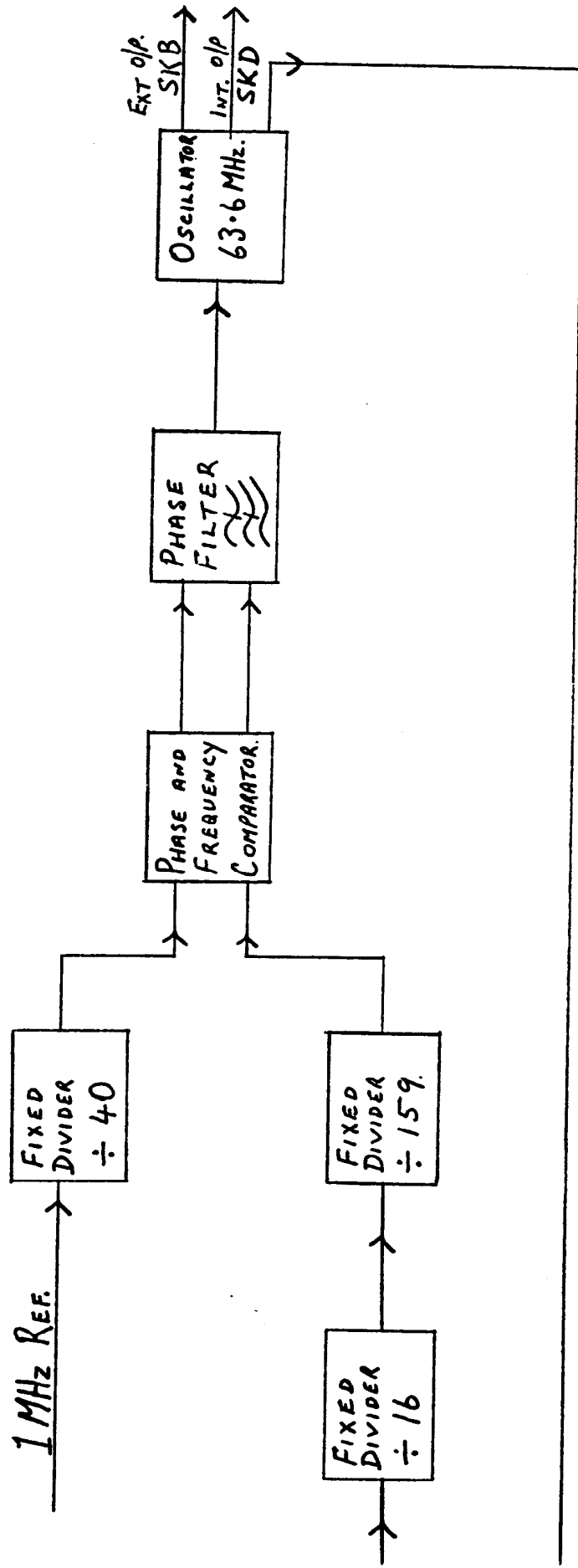
#### 10.4 2nd Local Oscillator

10.4.1 The fixed-frequency 2nd local oscillator is housed on panels K and L. It consists of a circuit of the form shown in Figure (a) with a divider in the reference input line. An output frequency of 63.6 MHz is produced.

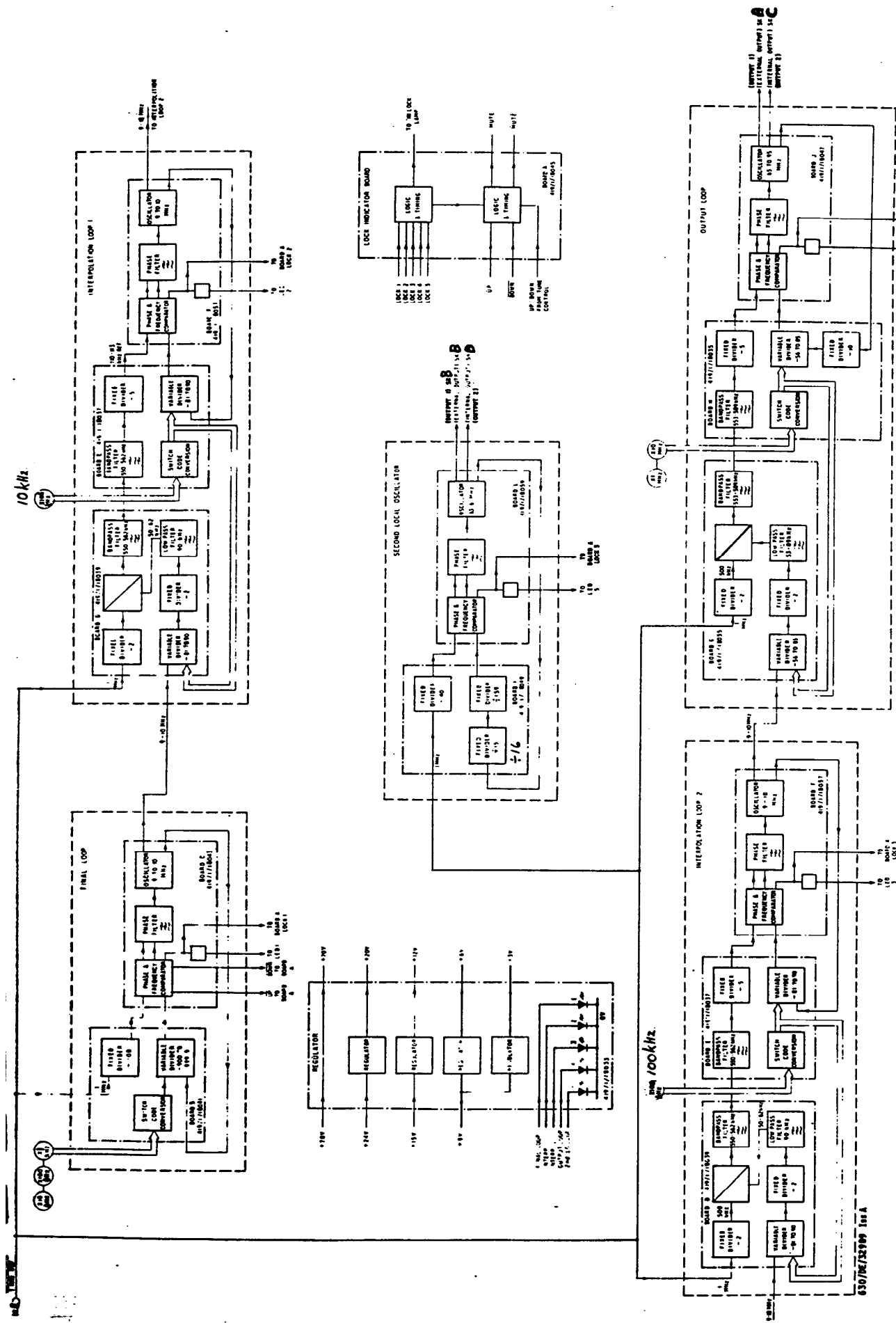
#### 10.5 Monitoring

10.5.1 A monitor output is taken from the Phase and Frequency Comparator of each phase-lock loop. A LED indicator is provided for each of the five loops, indicating when it is in lock. When all are in lock, a further LED indicator indicates 'all in lock'. When tuning (ie frequency variation) is in progress lock is lost; under these conditions a muting output is produced which shuts down the receiver outputs until lock is acquired on the new tuning setting. The monitoring circuits are housed in panel A.

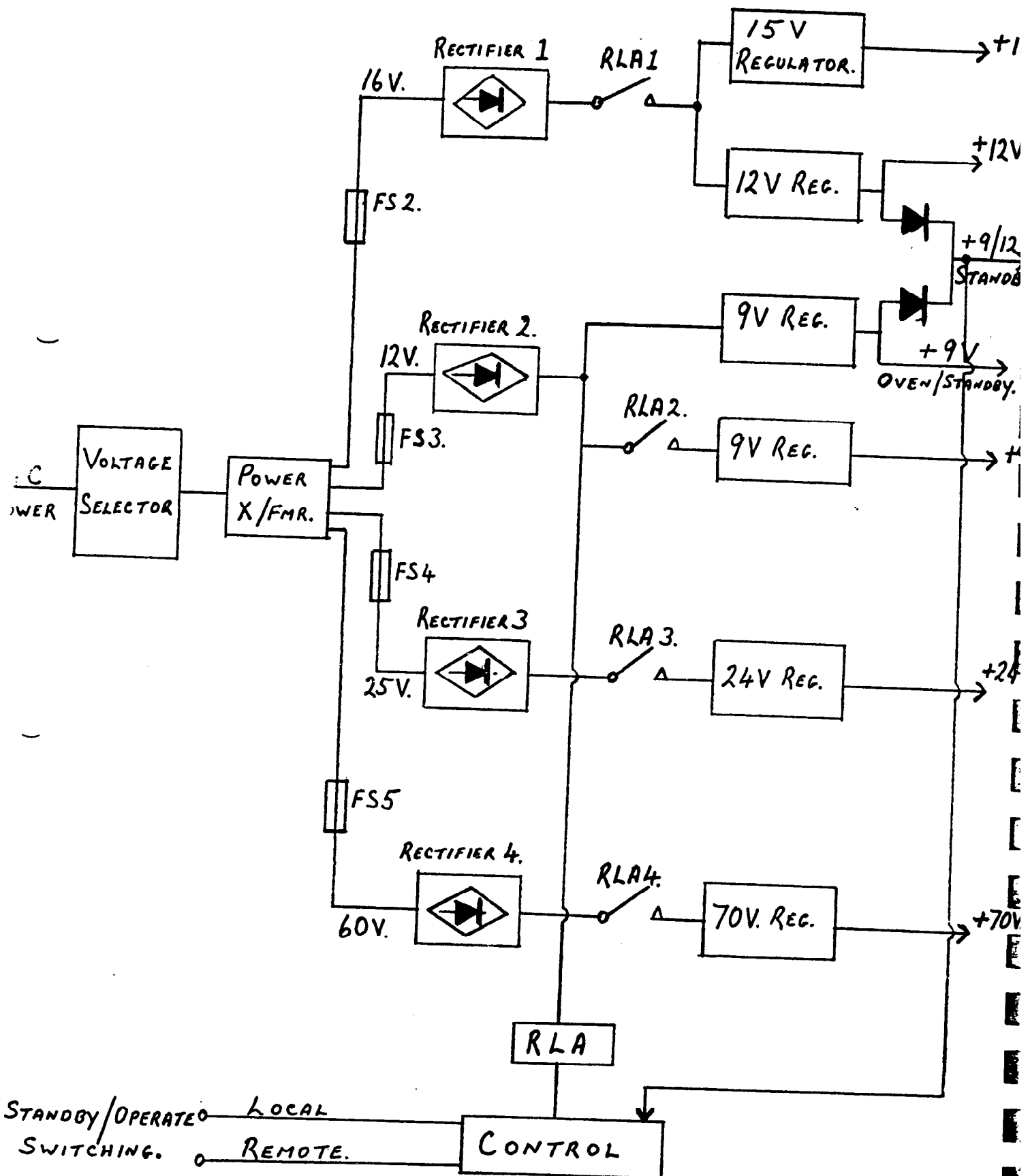
## SECOND LOCAL OSCILLATOR.



MODULE 9A: SYNTHESISER.



Module 9a overall functional block diagram

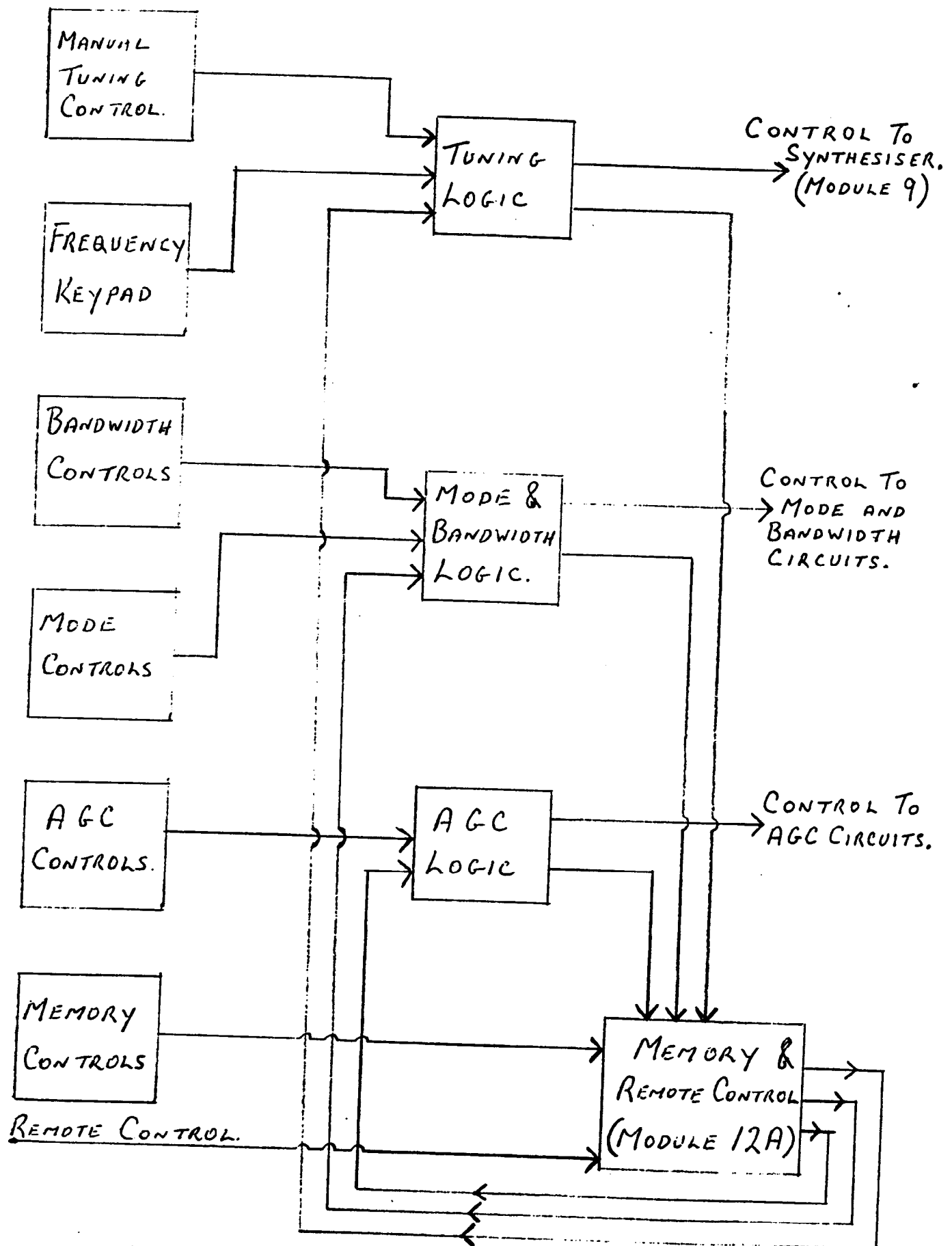


MODULE 8C: POWER SUPPLIES

## 11. MODULE 8C : POWER SUPPLIES

### 11.1 Functional Description

- 11.1.1 Module 8C is the Power Supply Unit, operating from a 45 to 400 Hz single-phase AC supply of either 100 to 125V, or 200 to 250V. Power consumption is approximately 90VA. DC power outputs are +9V, +12V, +15V, +24V and +70V.
- 11.1.2 Four bridge rectifiers are fed from the power transformer, each rectifier having a reservoir capacitor with discharge resistor and one or two voltage regulating circuits. In the receiver 'standby' stage, AC power is applied, Relay A is not energised, and only one of the 9V regulators gives an output (+9/12V STANDBY), this supplies the control logic circuitry. Relay RLA is powered by the raw 12V rectifier output and operated by the control logic.
- 11.1.3 On switching the receiver from STANDBY to OPERATE, RLA is energised and rectified DC is applied to the remaining five regulators, all DC outputs are then available. In addition, the +9V/+12V STANDBY output voltage rises from +9V to +12V.



MODULE 10J: BASIC FUNCTIONAL DIAGRAM.

## 12. MODULE 10J : FRONT PANEL AND CONTROL CIRCUITS

### 12.1 Introduction

Module 10 embraces the front panel of the PR 2250 receiver and the circuit-board mounted upon it. These two items together embody all the digital logic which forms the interface between the operator and the receiver proper. The logic operates in conjunction with the memory circuits in Module 12A.

### 12.2 Basic Functional Description

#### 12.2.1 Frequency Control

The operator controls frequency either by using the keypad or by use of the optical encoded manual tuning control. Provision is also made for recalling frequencies stored in the memory. These three sources generate the control input to the tuning logic. The tuning logic output determines the frequency of the synthesiser (1st LO). In addition, a frequency data output is fed to the memory circuits.

#### 12.2.2 Mode and Bandwidth Control

The mode and bandwidth controls are to a certain extent interdependent, in as much as selecting some modes automatically selects the appropriate bandwidth. However, where this is undesirable, the automatically selected bandwidth setting can be manually over-ridden. The mode and bandwidth logic also generates an input for the memory.

#### 12.2.3 AGC Control

AGC decay time-constant is operator selected. The selected value is fed to the AGC circuits and the memory.

## Module 10J: Keypad.

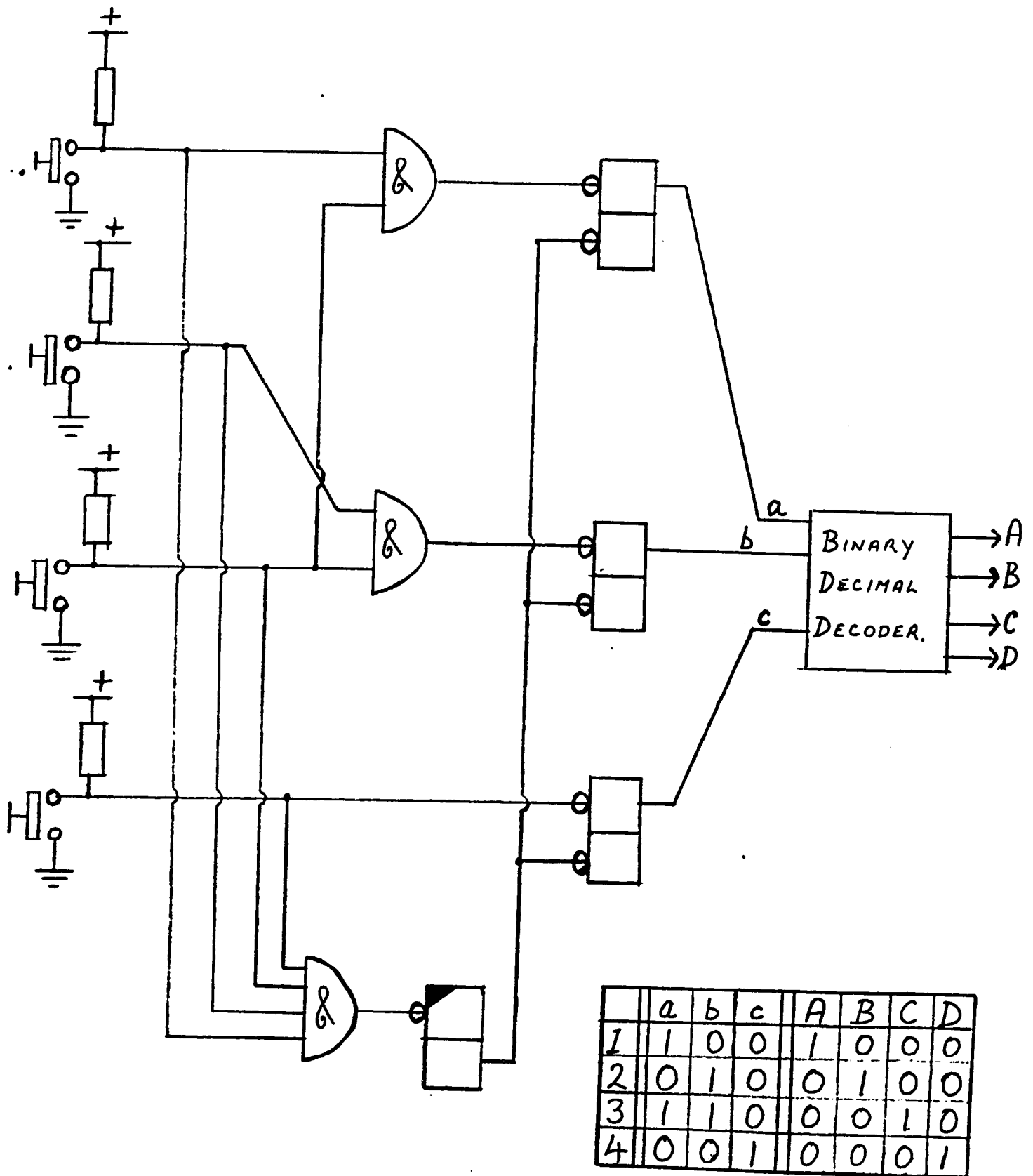


FIG (b) BASIC PUSH-BUTTON SYSTEM.

#### 12.2.4 Memory Control

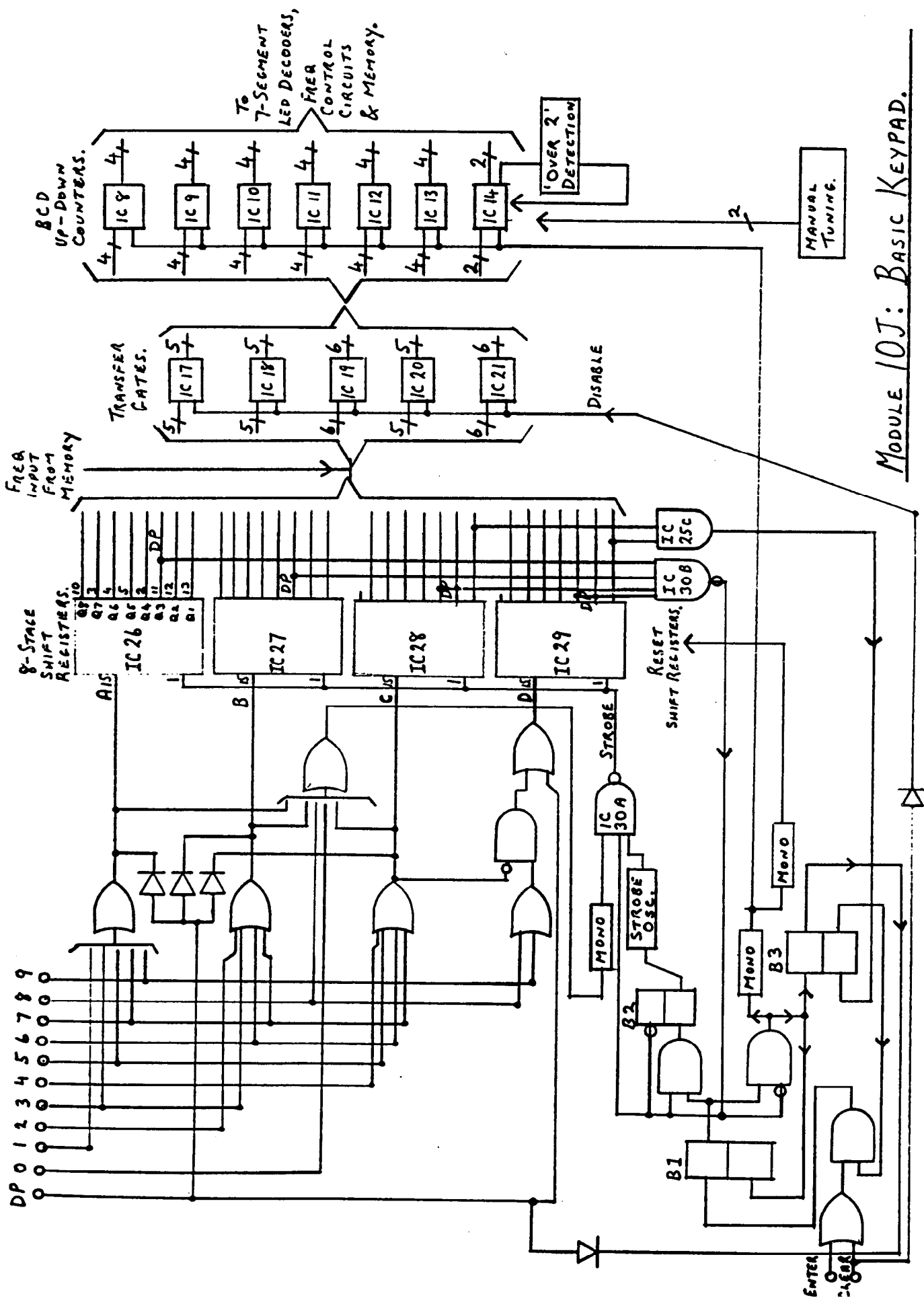
The memory has 16 storage channels. The memory is battery maintained, and will hold data for several months while the receiver is switched off. Recall facilities allow any stored set of data to be instantly applied to the receiver controls.

#### 12.3 Push Button Control

12.3.1 Apart from the manual tuning and some switches, all other operator controls are 'press to operate' buttons. The basic system can be seen in Figure (b). Operation of any button triggers the monostable, producing a very short '1-0-1' output pulse and also applying a '0' set level to one or more bistables. Those bistables which do not receive a '0' set level are reset by the short duration monostable output pulse, which ends before the operator releases the button. In the period between the end of the monostable output pulse and the button release, one or more bistables are set.

12.3.2 In Figure (b) a four-button circuit is shown. Button 1 produces binary 1 at a, b, c; Button 2 produces binary 2 and so on. The binary number set into the bistables is decoded to produce a '1' level on one output of the decoder. The system is applicable to any number of buttons by use of suitable "AND" gating and sufficient bistables to store the largest binary number required.

12.3.3 As an example, Push-Button 4 in Figure (b); the monostable produces a short '1-0-1' pulse which resets the upper two bistables. It cannot reset the lower bistable because of the '0' set level applied by Button 4.



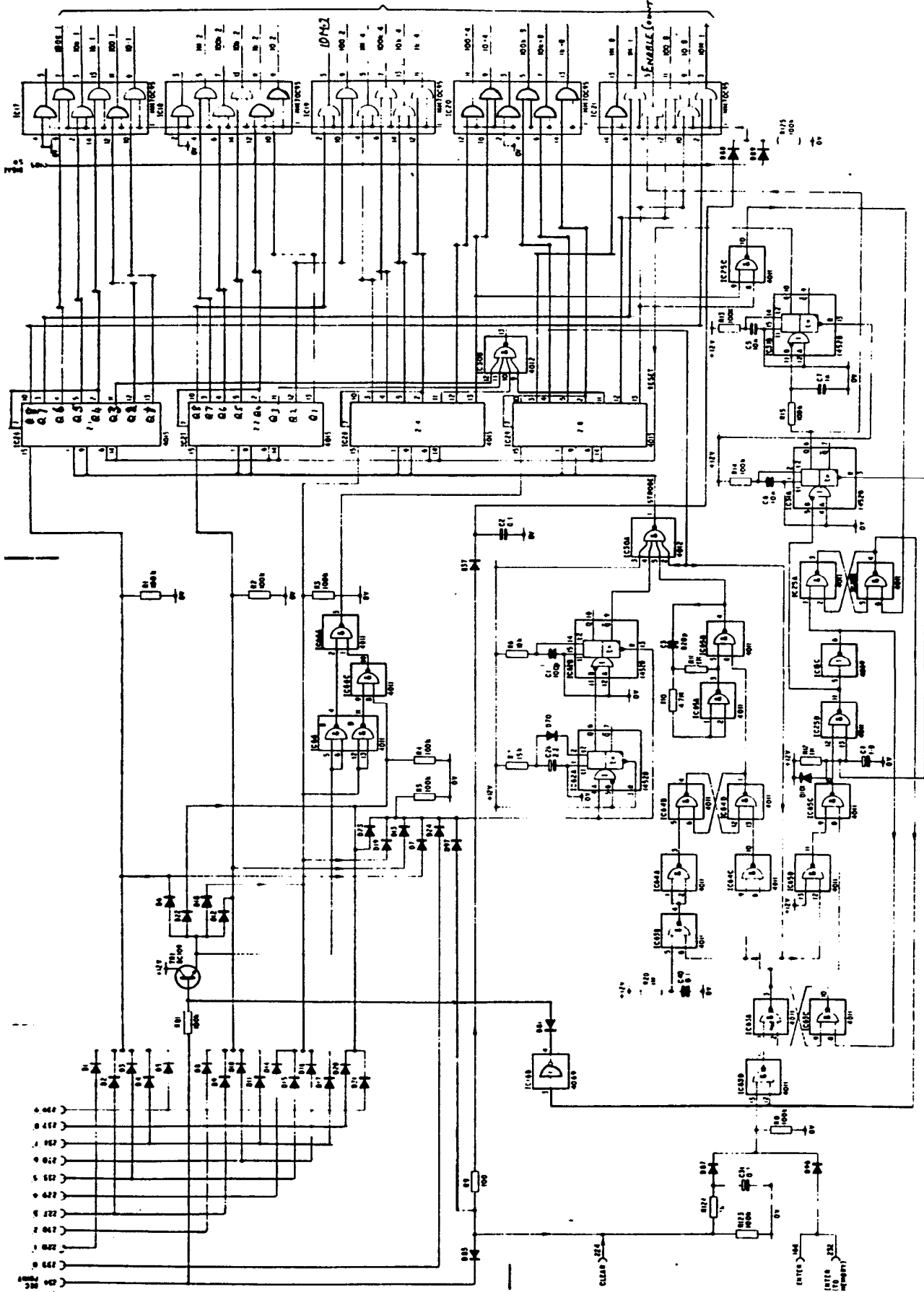
After the end of the monostable output pulse, the button will still be held. During this period, the lower bistable is set, producing a - 0, b - 0, c - 1 ie binary 4 in parallel form. This binary 4 will remain stored in the bistables until another button is pressed: it is decoded to produce a '1' output on line D.

## 12.4 Keypad

12.4.1 On entering a frequency on the keypad numerical inputs, a logic '1' is fed through one or more 'OR' gates consisting of three bands of diodes to four 8-stage shift registers. The shift registers are IC26, IC27, IC28 and IC29. The inputs and outputs of the shift registers are in binary form. The first binary output will appear at Q1 of the shift registers. On receipt of the next entry from the keypad the first output on Q1 moves to Q2 and the second entry takes up position on the Q1 output of the shift registers. With each succeeding entry the output of the shift registers moves up one place.

12.4.2 To make a valid entry on the keypad the decimal point must be activated. Depressing the DP button activates a transistor and this produces a logic '1' at the Q1 outputs of all four shift registers. A logic '1' appearing at the Q1 outputs of IC28 and IC29 is sensed by IC25C, and via various ICs and the write diode D81, the transistor is switched off and held off, thus preventing further operation of the decimal point key. Whether further numerical entries were or were not made after the decimal point entry does not affect the operation so, for simplicity, we will assume there were none.

12.4.3 The next operation is to press the ENTER button. This in conjunction with a level '1' (due to the decimal point) causes a STROBE PULSE from IC30A to CLOCK the





Shift registers. When the decimal point (1-1-1-1) reaches the Q3 outputs from the shift registers it triggers IC30B. IC30B output level drops from '1' to '0' and the strobe oscillator stops. The entries made on the keypad are now in the correct position in the shift registers to operate the display decoders and produce a meaningful output to the synthesiser. This is done via BCD UP/DOWN counters which, for keypad entries, merely act as stores.

- 12.4.4 At the same time as the strobe oscillator stops, the combination of IC30B output at '0' and IC63A output at '1' has three effects:
- (1) The two monostables, IC31A and IC31B are fired. The first one applies a preset to the up-down counters (IC8 to 14) allowing the register outputs to appear on the counter outputs. The transfer gates IC17 to IC21 are normally transparent to data. There is delay on the second monostable which, a little later, resets the shift registers ready for the next entry.
  - (2) IC63A output is set to '0' which is the start state for another operation.
  - (3) IC25B output is set to '0' which removes the 'hold' from the transistor in the decimal point line which is the start state for another operation.

- 12.4.5 The connection between the shift registers and the up-down counters is made via transfer gates which are normally transparent to data. Their function is to break the connection when clearing an erroneous keypad entry. If, after a keypad numerical entry has been made but before the ENTER button is operated, it is desired to 'start again', the CLEAR button is

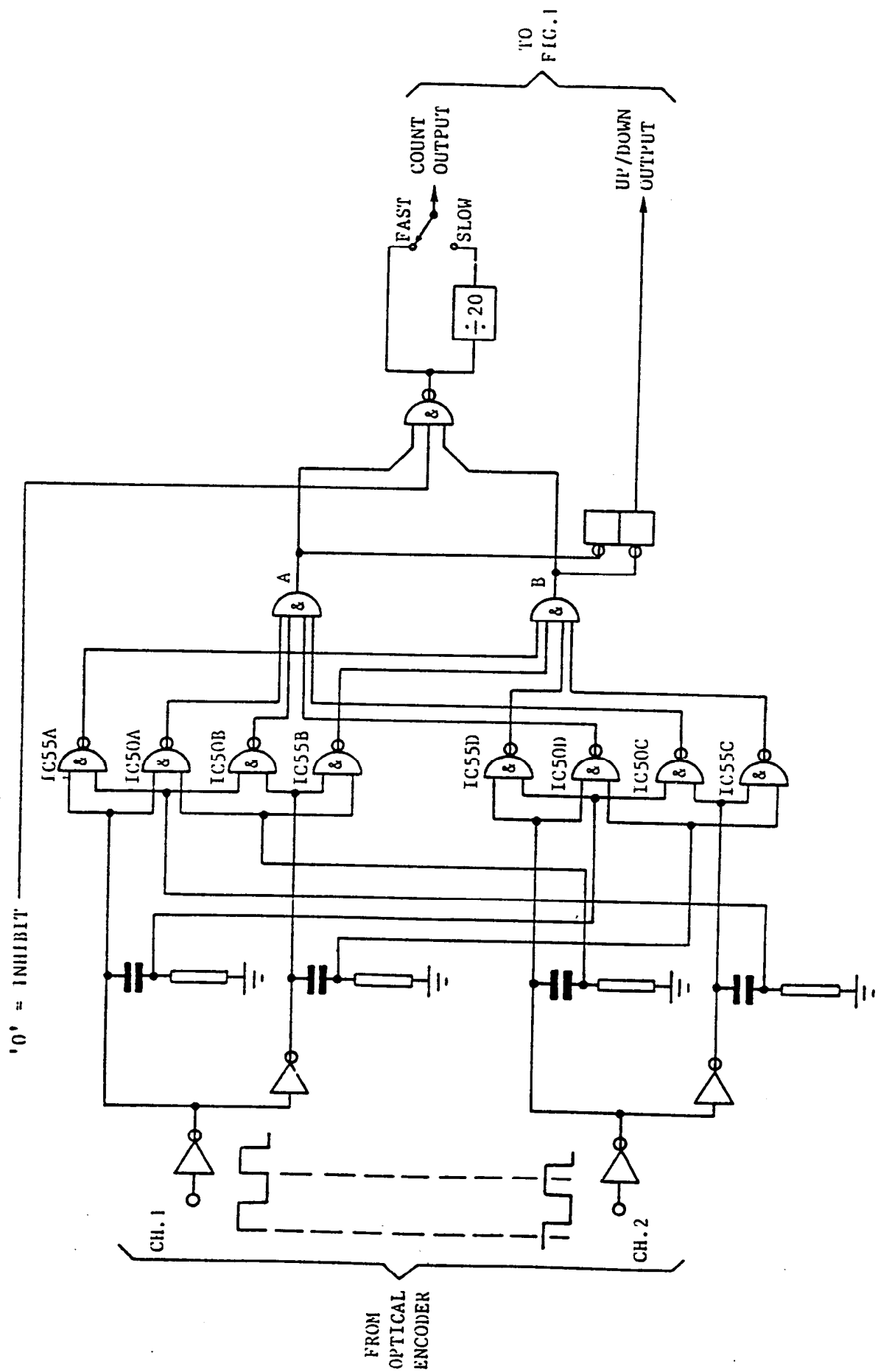


FIG (e) BASIC MANUAL TUNING LOGIC

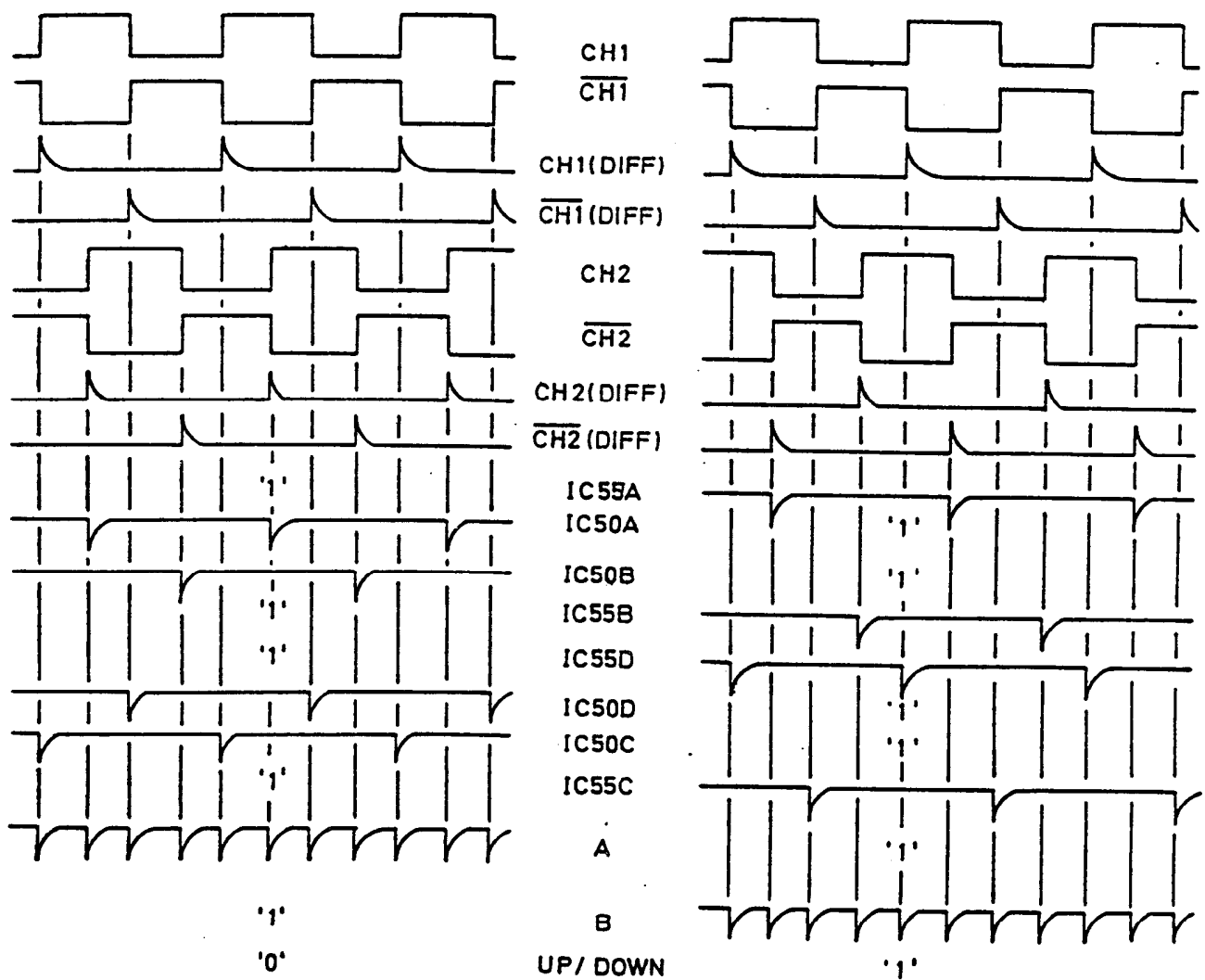


FIG (f) MANUAL TUNING CIRCUIT ACTION

pressed. This functions exactly as the enter button but with one additional action, which is to disable the transfer gates and prevent the incorrect entry from appearing at the counter outputs.

- 12.4.6 The up-down counters consist of IC8 to IC14. IC14 of the counter deals with the '10 MHz' digit. This must not exceed 2, as the maximum frequency is 29.99999 MHz. An 'over 2' detector comprised of IC15C and IC15D senses the output from IC14: if it exceeds binary 2 due to incorrect keypad entry, then the detector resets IC14 to bring its output within the range of the receiver.
- 12.4.7 The outputs of the up-down counters are in parallel BCD, and define the frequency in kHz. The output controls four functions.
- (1) THE SYNTHESISER FREQUENCY CONTROL UNIT (MODULE 9A)
  - (2) LED DECODERS OF THE FRONT-PANEL FREQUENCY DISPLAY (MODULE 10J)
  - (3) MEMORY CIRCUITS OF MODULE 12A
  - (4) FILTER-SWITCHING LOGIC CONTROLLING MODULE 1 (NOT USED)
- 12.4.8 The outputs from the up-down counters are fed out of Module 10J to the memory circuits and the frequency control circuits. Inside Module 10J they are applied to seven BCD 7-segment LED decoders (IC1 - IC7). These devices drive the front-panel frequency display. The decimal point on the display is a separate LED which is permanently illuminated via R57.

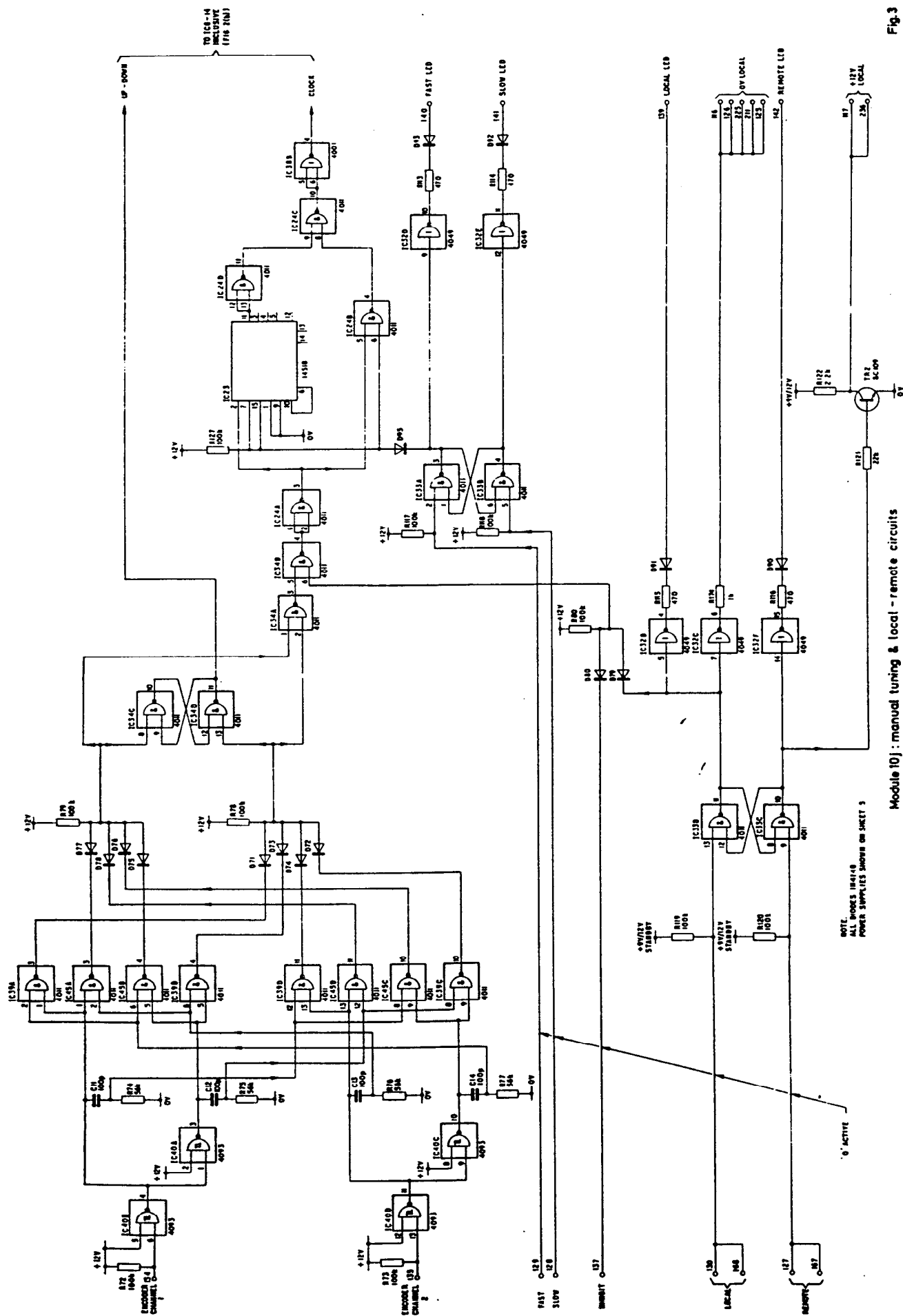


Fig.3

## 12.5 Manual Tuning

12.5.1 The optical encoder is driven by the manual tuning knob and uses a 12V d.c. supply to produce two square-wave outputs, 'Channel 1' and 'Channel 2': these outputs have a 90° phase relationship and at worst case, have a '1' level value of +12V and a '0' level value of 0.3V nominal. On each channel, 500 pulses are produced per encoder revolution.

12.5.2 The two outputs from the encoder are 'cleaned' by trigger inverters IC40B and IC40D. Two further trigger inverters IC40A and IC40C provide inverted signals. The output from each of the four trigger inverters is applied to a CR differentiation circuit. Each of the two encoder outputs is therefore available in four forms:

- (a) Direct
- (b) Inverted
- (c) Direct differentiated
- (d) Inverted differentiated

This produces a total of eight inputs to a gating circuit formed by IC39 and IC45 together with diodes D71-D78. Two outputs are always produced: one is a train of '1-0-1' short pulses at four times encoder output pulse rate, while the second is a steady '1' level (Points A and B in Figure (c)). Reversal of control rotation direction reverses the two states. The two outputs are applied to a set-reset bistable and to a NAND gate. The bistable output level indicates direction of rotation, while the pulse train indication of rotational speed and quantity appears at the output of the NAND gate.

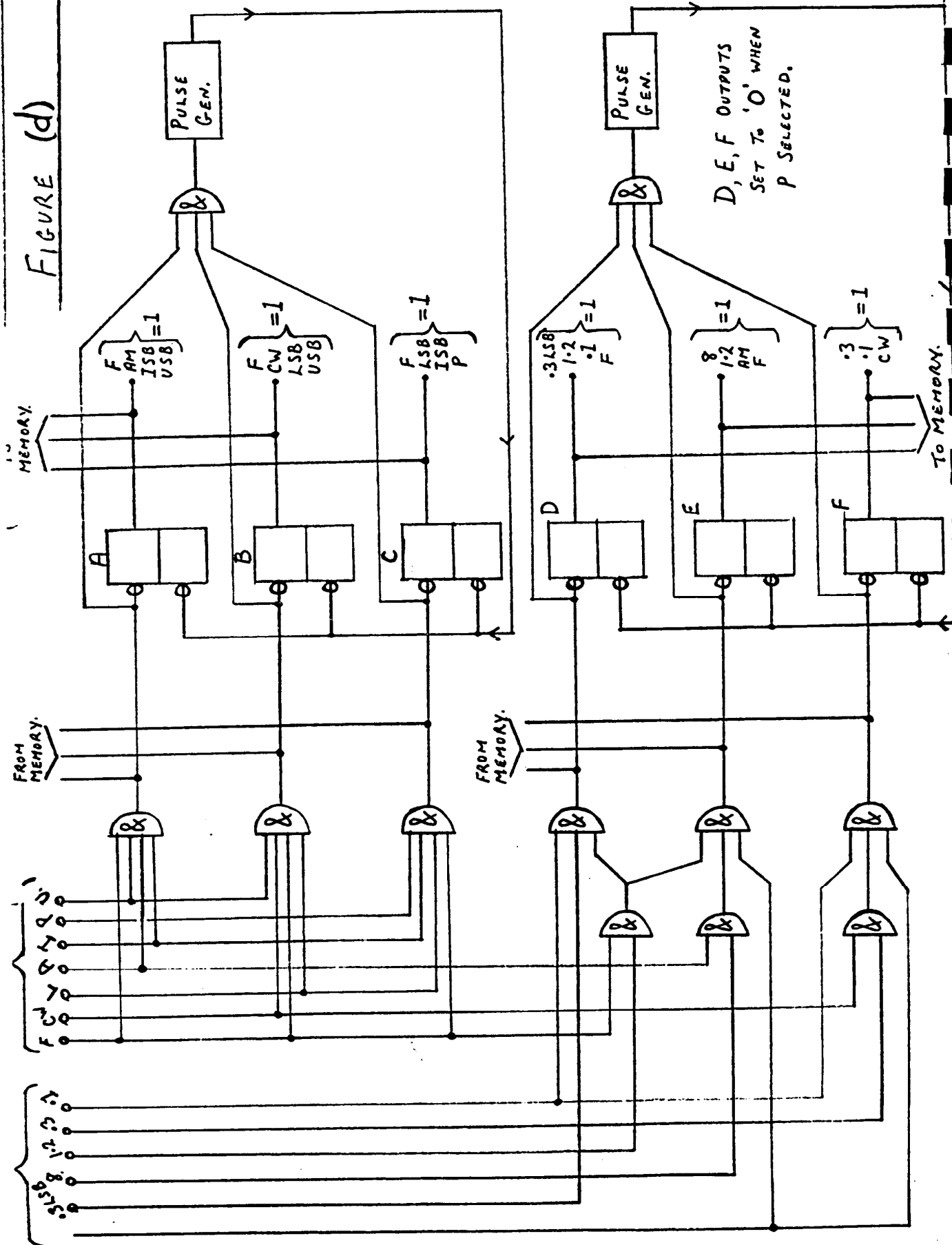
12.5.3 The output from the bistable is fed to the up-down inputs of IC8 to IC14, while the output from the NAND gate is applied to the clock inputs of IC8 to IC14. According to direction of control rotation, the numbers stored in the counters can be increased or decreased, so controlling the counter output values.

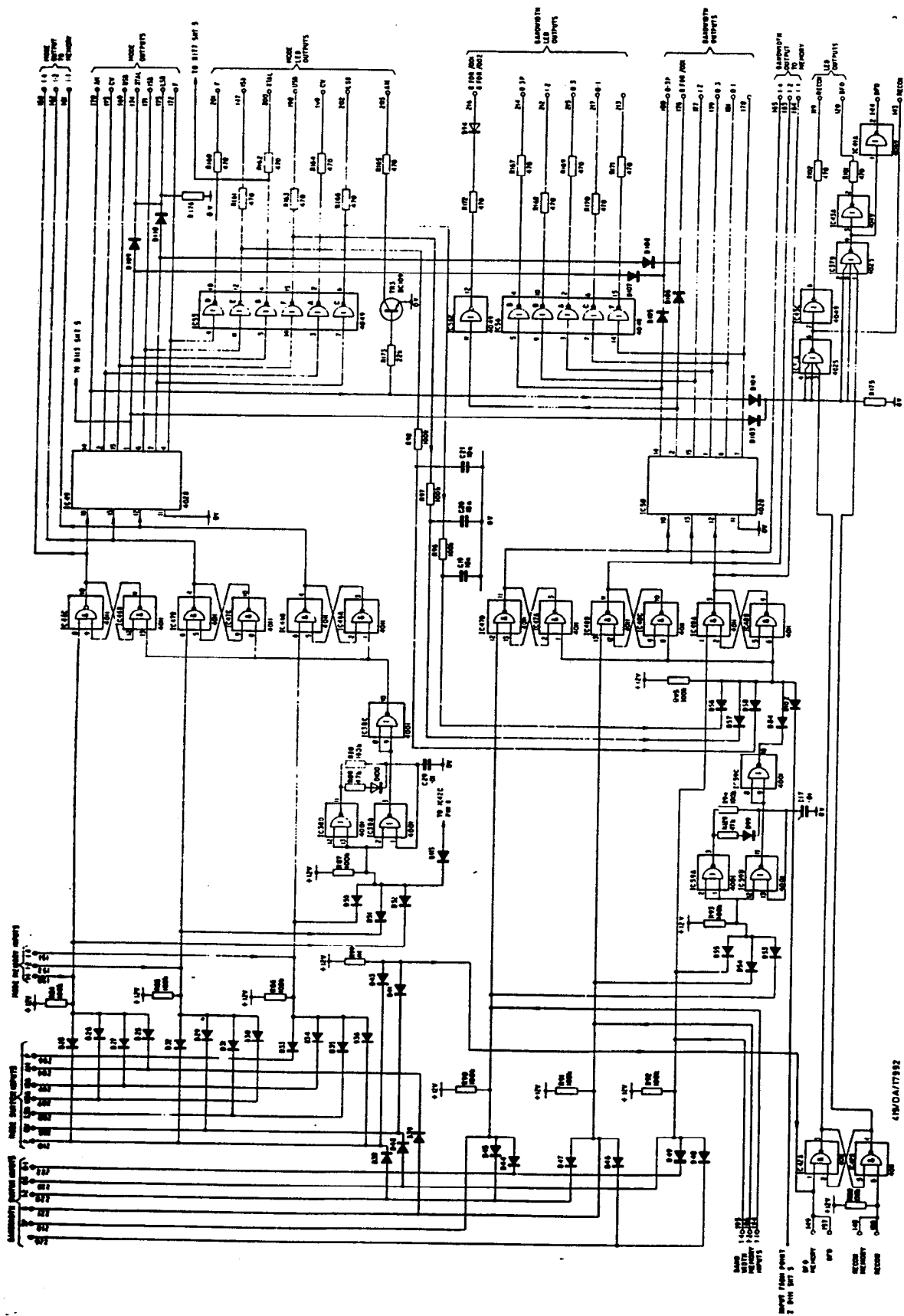
## 12.6 Mode and Bandwidth Control

- 12.6.1 The Mode and Bandwidth control circuit is a straightforward extension of the basic circuit shown in Figure (b). Two groups of press-buttons are employed, one for mode (F, CW, LSB, USB, ISB, AM, P) and one for bandwidth (8, 1.2, 0.3, 0.1 kHz). Each group is gated into three bistables. The two groups of inputs can be produced either by the front-panel buttons or from the memory.
- 12.6.2 The operation of the F, CW or AM mode buttons automatically sets up a particular bandwidth. However, this does not prevent subsequent selection of a different bandwidth.
- 12.6.3 Operation of the P mode button automatically selects 0.3 LSB bandwidth. The bandwidth, AGC and reconditioned carrier LEDs are extinguished. The preset conditions cannot be over-ridden.
- 12.6.4 A basic block diagram of the circuit can be seen in Figure (d). The two groups of bistables each produce a 3-bit binary number output which is decoded by the controlled circuits.
- 12.6.5 The functional diagram shown in Figure (d) omits one input to the basic circuit; this input is an inhibit on bistables D, E and F, which comes into operation when USB, LSB, ISB or P mode is selected. An '0' level output is taken from the mode LED outputs and fed via diodes D56, D57, D58 and D102 (see Figure 4, Chapter 10 Service Manual) and is applied as a permanent inhibit to the three bandwidth selection bistables for as long as the mode remains selected.

Note that, if during USB, LSB, ISB or P mode operation a bandwidth button is pressed it will select

FIGURE (d)





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Fig 4'

the appropriate circuit but will only do so while the button is pressed; this is not a valid mode of operation and is only mentioned to avoid this effect being mistaken for a fault condition.

12.6.6 Each of the two groups of bistables supply the inputs to a BCD - decimal decoder (IC49 and IC50). The output lines from each decoder are normally at '0'. One output line level rises to '1' according to the inputs applied.

12.6.7 The outputs from the decoders are the controlling inputs to the Mode and Bandwidth circuits, and are also fed via LED drivers IC55, TR3 and IC56 to operate the front-panel LED indicators. The mode and bandwidth outputs to the memory circuits are taken in parallel with the inputs to the decoders.



## 12.7 AGC Control

- 12.7.1 As in the mode and bandwidth control circuits, the AGC selection circuit also uses push-button controlled bistables, Figure (e).
- 12.7.2 On operation of the AGC control button a level '0' is applied to the appropriate bistable A, B or C. The combined binary output is decoded by four AND gates, the outputs being fed to the control circuits, and to the front-panel LED indicators.
- 12.7.3 In mode 'P', SHORT AGC is automatically selected via IC49 and D113 (Service Manual, Chapter 10, Figure 4). The 'P' mode LED output - level '0' - is also applied via D111 to bistables A, B and C. This sets the bistable outputs to logic '0' and the AGC LEDs are extinguished.



**Module 10 J: AGC & power circuits**

**Fig. 5**

