5. TECHNICAL DESCRIPTION

5.1. Mechanical

The receiver is built on a rugged zinc plated and passivated iron chassis.

The receiver contains 14 printed circuit boards. Six of these: /207\, /208\, /209\, /210\, /212\ and /M 220\ or /S 220\ are plug-in boards which are placed in a special screened box at the right hand side of the receiver chassis and contains circuits for the AF-amplifier and the synthesizer. Th rest of the circuit boards except /211\, /213\ and /228\ are housed in rive screening cans. The can at the left hand side of the top compartment contains the 2nd mixer /S 203\ and the IF-amplifier /205\ while the can in the middle contains the IF-filters /M 217\. In the bottom compartment, the screening can contains the input filters and 1st mixer /216\. Finally, in the front compartment behind the front panel, switches are located together with the display and keyboard /211\, the filter board /213\ and the noise generator /228\. This compartment also contains the loop 3-divider /214\ and the 3 MHz lock /293\ in their separate screening cans. The front panel is electrically insulated from the chassis. This feature permits connecting the chassis to a separate earth when the receiver is mounted in the same rack with a transmitter.

5.2. Circuit Discription, General

Each of the printed circuit boards and also the chassis mounted components in this equipment have been allocated an identification number between /201\ and /293\. The designation of a component or terminal includes this number as a prefix, e.g. 213R3 (resistor R3 on board /213\) or 213-3 (terminal No. 3 on board /213\).

For convenience in this section and on the circuit diagrams the prefix is omitted except where there is a risk of ambiguity.

The circuit diagram is divided into a wiring diagram on page 8-4[illegible] showing interconnections between the printed circuit boards, and circuit diagrams of the individual printed circuit boards. The mode of operation follows the block diagrams on pages 8-46, 8-47 and 8-48 showing the signal path, the frequency synthesizer and the frequency selection, respectively.

5.3. Circuit Summary, Signal Path

The incoming signal is fed via a low-pass filter on board /213\ and BAND switch on board /216\ to the RF Input Filters. The board also contains the 1st mixer stage that converts the input signal frequency to the 1st intermediate-frequency 38 MHz by mixing it with a signal from the Frequency Synthesizer. Before leaving the board the intermediate-frequency signal passes a crystal filter which determines the double-sideband selectivity of the receiver.

The 1st intermediate-frequency signal is fed to the 38 MHz Bandpass Filter /221\ where spurious responses, if any, are further attenuated. The signal is passed on to the 2nd mixer on board /S 203\, where it is converted to the 2nd intermediate-frequency, 1.4 MHz by mixing it with a signal derived on basis of the 11.2 MHz TCXO on board /M 220\ or /S 220\ and the 3 MHz clarifier oscillator signal on board /S 203\.

The 2nd intermediate-frequency signal is fed to the IF-filters on board /M 217\. The selection of the desired filter is carried out by the BANDWIDTH switch.

On the IF-Amplifier board (205) the signal is amplified and detected and the audio frequency output is fed to the VOLUME control via an active low-pass filter.

The audio-frequency signal is amplified on plug-in board (M 220) or (S 220) which also contains the line-amplifier and TCXO.

5.4. Circuit Description, Signal Path Boards

5.4.1. (216) Input Filters

The PRESELECTOR RANGES consist of six bands, each tuned with the variable capacitor C5. The 3 bands from 0.06 MHz to 1.6 MHz consist of the coils T11, T12 and T13 and associated components. The 3 bands from 1.6 MHz to 30 MHz consist of six coils which two by two, together with the remaining components, constitute a double band-pass filter. The 2 bands, .18 - .53 MHz and 1.6 MHz - 4 MHz are, in the positions 500 kHz and 2182 kHz fixed tuned with capacitors C3 and C1, C2, C4, C6 respectively. In the DUPLEX ranges all circuits are fixed tuned. The seven DUPLEX filters comprise three tuned circuits, and their selectivity is high to provide effective attenuation of ones own transmitter. All the filters in the PRESELECTOR and the DUPLEX range have a balanced output for the mixer.

For the 0.01 - 1.6 MHz range there is a low pass filter consisting of L4 and C46.

Switching of the filter outputs is performed by a DC voltage which controls the diode switches at the balanced filter outputs.

The 1st mixer, which is double balanced, consists of the matched field effect transistors TR1, TR2, TR3 and TR4. The 38 MHz output is fed to the 2nd mixer via a 38 MHz crystal filter.

5.4.2. (S 203) 2nd Mixer

This board contains the 2nd mixer, the clarifier oscillator and mixer and finally a 38 MHz input attenuator.

The 2nd mixer consists of field effect transistors TR5 and TR7. The 1.4 MHz output is connected to the IF-Filter board (M 217). The injection signal for the 2nd mixer is obtained by mixing a 33.6 MHz and a 3 MHz signal in the integrated circuit IC1. The 33.6 MHz signal is derived from the TCXO on board (M 220) or (S 220), while the 3 MHz signal is obtained by using TR1 as a crystal oscillator. The frequency of the 3 MHz oscillator can be varied from the CLARIFIER control by means of the variable capacitance diode D1-4. When the CLARIFIER control is set to off position the control is out of circuit and the 3 MHz signal is faselocked to the TCXO by means of the 3 MHz Lock board (293) in order to obtain the maximum stability of the receiver. The 36.6 MHz output from IC1 is filtered and amplified in TR4 before being applied to the 2nd mixer. The 38 MHz input attenuator consists of the PIN-diode D5 and associated components. The current in the PIN-diode is controlled by TR6, the base of which is connected to the AGC-voltage on board (205). The 38 MHz input frequency is stepped up in a transformer before being applied to the mixer input.

5.4.3. (M 217) IF-Filters

The IF-Filters consist of four 1.4 MHz crystal filters and a 1.4 MHz WIDE filter consisting of the coils L1 and L2 and the capacitors C2, C9 and C11. The selection of the correct filter is made by the BAND-WIDTH switch which controls the diode switches at the filter input and output.

When the BAND Switch is in position 500 kHz or 2182 kHz the 1.4 MHz WIDE filter is automatically selected.

5.4.4. (205) IF-Amplifier, Detector and AGC

The IF-amplifier consists of transistors TR1 and TR2. A 1.4 MHz Band-pass filter connects the amplifier to the signal detector IC1. This integrated circuit contains a balanced mixer and a high-gain limiting amplifier. The signal voltage is applied balanced to the one input port of the mixer, terminals 7 and 9, of the integrated circuit.

When the detector works as an AM detector the signal voltage is also fed to the amplifier input terminal 14, via D 12. This signal is amplified and clipped to constant amplitude and internally connected to the other input port of the balanced mixer where it is mixed with the modulated signal. The difference frequency, which contains the wanted AF-signal, is taken off at the mixer output, terminal 8. The AF-signal is then fed to an active low-pass filter consisting of transistor TR5 and associated components.

In the A1/F1 mode and the A3J/A3A mode D12 is blocked while D11 is conducting and the 1.4 MHz signal from the AF-amplifier, board (M 220) or (S 220) is now fed to the amplifier input. The mixer is working in the same manner as before except that now the 1.4 MHz signal is the re-inserted carrier.

Also the sum frequency of the input signals is present at the mixer output. This signal is used for automatic gain control and is taken off across the 2.8 MHz tuned circuit. It is amplified in TR4 and rectified in the AGC detector TR3. The current of TR3 increases for increasing signal level causing the collector voltage to drop. The collector is connected to the bases of the IF-transistors and a lower collector voltage means reduced gain in the IF-Amplifier.

The AGC time constants are determined by C2 and C8. The circuit combines a short attack time and a long decay time. The resistor R11 in series with C8, which mainly determines the decay time, prevents short noise pulses from giving a long decay time.

The gain can also be controlled manually by means of the SENSITIVITY control which in combination with the diode D1 determines the maximum collector voltage of TR3 and with that the highest available gain of the IF-amplifier.

The AGC switch switches off the AGC by disconnecting the emitter current of TR4. The base voltage of the IF transistors is then controlled only by means of the SENSITIVITY control.

5.4.5. /M 220\ or /S 220\ AF-Amplifier

The board contains the AF amplifier, the line amplifier, the BFO and the TCXO. The AF amplifier is an integrated circuit provided with a built-in thermal limiting circuit and protection against accidentals short circuit of the output. The line amplifier consists of the transistors TR1 and TR3. The BFO signal is obtained by using part of IC1 as a crystal oscillator. The frequency of the 12.6 MHz oscillator can be varied from the BFO control by means of the variable capacitance diode D3. The 12.6 MHz signal and the 11.2 MHz TCXO signal are then mixed in the integrated circuit IC1 to obtain a 1.4 MHz signal for the detector on the board /205\ The TCXO frequency 11.2 MHz is amplified in TR2 and TR6 and clipped in TR10. The signal is then divided by 8 to 1.4 MHz in the integrated circuit IC3. From the output of the divider a 1.4 MHz signal is fed to the 3 MHz Lock board /293\. Another 1.4 MHz signal from the divider is fed to the Mother Board /201\.

The TCXO frequency is amplified in TR6, TR9 and TR10, and the third harmonic is taken off in the filter consisting of coils T2, T3 and associated components. The 33.6 MHz signal is fed to the 2nd MIXER on board /S 203\.

In the /M 220\ in R 5001 version S-1 it is possible when the resistor R1 is unsoldered and the coax-cable is mounted as shown on the diagram page 8-65, to make use of an external master oscillator for improving the stability of the receiver.

5.4.6. /213\ Filterboard

The Filterboard contains three voltage regulators, IC1, IC2 and IC3. IC1 supplied 12V to the synthesizer, while IC2 supplies 12V to the other parts of the receiver. IC3 supplies 5V to the synthesizer and other logic circuits.

RF filters are inserted in the power supply, muting and AF output lines in order to suppress noise and interference on these lines.

The Filterboard also contains a low-pass filter for the aerial input, to prevent the radiation out of the receiver.

5.4.7. /228\ Noise Generator

To ease the setting of the preselector the receiver incorporates a Noise Generator.

The Noise Generator consists of a three-stage noisy amplifier generating a wideband noise.

When the preselector button is pushed the Noise Generator is switched on and connected to the Input Filters /216\. Automatically the AGC is switched on.

5.5. Circuit Summary, Frequency Synthesizer

This Frequency synthesizer consists of two programmable phase locked loops (Loop 1 and Loop 2), the outputs of which are controlling a third (Loop 3) from which the complete synthesized signal is derived and fed to the 1st mixer in the signal path.

The output frequency of Loop 1 is controlled by the 100 Hz, 1 kHz and 10 kHz information according to the contents of the displays provided the receiving mode chosen is not F1. If the F1-mode is chosen the output frequency is decreased by 30 kHz, which means that the final output frequency of the Synthesizer is decreased by 1.5 kHz.

Loop 1 produces an output frequency in 999 steps from 20.000 MHz to 21998 MHz in all modes but F1. In the F1-mode it is from 19.970 MHz to 21.960 MHz. This frequency is divided by 200 and serves as a variable reference frequency for the Loop Translator.

Independent of the different receiving modes Loop 2 is controlled by the 100 kHz, 1 MHz, and 10 MHz information according to the contents of the displays. The output frequency of this loop is variable from 3.70 MHz to 6.69 MHz in 299 steps and is fed to the mixer of the Loop Translator, where it is subtracted from the synthesizer output frequency divided by 10, and finally compared with the variable reference frequency from this loop by means of Phase/Freq. Detector 3. A Frequency Comparator ensures that the Synthesizer output frequency divided by ten is higher than the output frequency of Loop 2. If this was not the case it would lead to a stable, unlocked condition of Loop 3.

The Frequency Synthesizer is locked to a 1.4 MHz signal derived from the TCXO, so that the output frequency will exhibit exactly the same stability as specified for the TCXO.

Provided that the 3 loops are locked the following equations, where fvcoi is short for output frequency of VCOi, will become valid:

Assumption: Receiving frequency is (ab, cde.f)kHz and MODE selected not F1 .

$(fvco_3 - 10) - fvco_2 - 200)$.

$fvco_3 = 10x(fvco_2 + (fvco_1 - 200))$

where

$fvco_1$ = (20000 + (d e f) x2) kHz and

$fvco_2$ = (3700 + (a b c) x 10) kHz and

$fvco_3$ = 38000.0 kHz + a b c d e.f kHz

5.6. Circuit Description, Frequency Synthesizer

5.6.1. /207\ Frequency Dividers

There are three divider chains, their associated buffer amplifiers, and two phase/freq. detectors are located on this board.

The Reference Divider produces the 2 kHz reference frequency for the Phase/freq. Detector 1, and the 10 kHz reference signal for the Phase/Freq. Detector 2, from a 1.4 MHz signal derived from the TCXO on board /M 220\ or /S 220\ .

The variable divider chains are composed of programmable up-counters and their associated external gating logic. The dividing action is accomplished by presetting (programming) these counters with the data blocks corresponding to the contents in the displays, at the end of each counting cycle. The data blocks contain the BCD 9's complement code of the corresponding digit.

In the Loop 1-Divider chain the F1 information is used to control the associated external gating logic. In the F1-mode this chain counts 15 clockpulses less that in any other mode, before concluding a counting cycle, thus the contents of the data blocks are independent of the mode.

The Loop 2-Divider chain counts independent of the receiving mode and adds, by means of the external gating logic, 370 extra clock cycles to what is determined by the three most important digits, before concluding a counting cycle.

The outputs from the variable dividers are led to their respective phase/freq. detectors and are here compared to the fixed reference frequency. In case of a frequency difference the detector will produce a DC error voltage which will adjust the associated VCO to establish the wanted frequency equality.

5.6.2. /208\ Loop Translator

This circuit board contains one half of Loop 3, namely the Frequency Comparator, the 200 divider, the Loop 3 Mixer, with its associated 1.5 MHz Low-Pass Filter, and Phase/Freq. Detector 3.

The VCO_1 output frequency is divided by 200 and fed, as a variable reference frequency, to one of the two input ports of Phase/Freq. Detector 3. The output frequency of VCO_3 divided by 10 is fed to the Loop Mixer, whose other injection signal is derived from VCO_2. The sum frequency from this mixing process is removed in a 9-order 1.5 MHz Low Pass Filter, thus only allowing the difference frequency to pass on via the following Buffer Amplifier, to the other port of Phase/Freq. Detector 3. This detector is almost identical to the detectors mentioned in the description of board /207\.

If the VCO_2 output frequency is higher than the Synthesizer output frequency divided by 10 at the beginning of an acquisition of Loop 3, this loop will end in a stable, unlocked condition. To avoid this these two frequencies are compared. If the frequency of VCO_2 is higher then the monostable multivibrator IC13 is triggered by the latch following the two divider chains and via the Phase/Freq. Detector 3, the frequency of VCO_3 is forced to rise, thus pulling Loop 3 out of this unwanted condition.

The output pulse from the detector is smoothed by means of a simple RC-filter before leaving this circuit board.

5.6.3. /209\ VCO_1 and VCO_2

The Loop Filter and Voltage Controlled Oscillator of both Loop 1 and Loop 2 are located on this board.

Both of these filters are active 3rd order low pass types with an integrated function incorporated. The purpose of the loop filters is to remove the pulses from the output of the Phase/Freq. Detector and allow only the DC-Information to pass on to the vari-cap diodes of the Voltage Controlled Oscillators. By use of the Phase Error Adjustment potentiometer the phase error pulse width can be minimized. Once adjusted this width will remain unchanged throughout the whole frequency range of the VCO, due to the use of an integrator in the Loop Filter. Both of the VCO's are amplitude regulated.

The selection of one of the three bands, in which VCO_2 is operating, is carried out by means of a decoding circuit on /212\.

5.6.4. /210\ VCO_3

This circuit board contains the Loop 3-filter and the Voltage Controlled Oscillator VCO_3.

The Loop 3-filter consists of a 1st order low pass filter and an integrator. The filter serves to remove the pulses of the Phase/Freq. Detector output signal and allow only the DC-information to pass on to the vari-cap diodes of VCO_3. By use of the Phase Error Adjustment the phase error pulse width can be minimized, and once adjusted it will remain unchanged throughout the whole frequency range of VCO_3 due to the use of an integrator in the Loop Filter.

VCO_3 consists of three Voltage Controlled Oscillators VCO_{3x}, VCO_{3y} and VCO_{3z}, each covering a band of approximately 10 MHz. The band selection is carried out by means of a decoding circuit on /212\.

The VCO_3 output signal is amplitude regulated and serves as an injection signal to the 1st mixer in the receiver signal path.

5.6.5. /214\ Loop 3-Divider

The Loop 3-Divider divides the frequency of VCO_3 by 10; this signal is then fed to the Loop Translator.

5.6.6. /203\ 3 MHz Lock

The 3 MHz Lock consists of two dividers, a phase/freq. comparator and a filter.

The 3 MHz signal from the clarifier oscillator on board /S 203\ is divided by 15 in the divider IC2 and compared in the frequency and phase detector IC3 with the 1.4 MHz frequency derived from the TCXO on board /M 220\, /S 220\ divided in IC1 by 7.

The output from the phase/frequency detector is amplified in TR4 and filtered in the low-pass filter R18, R19 and C8 and passed on to the VCXO on board /S 203\ when the clarifier/BFO control is set in off position.

5.7. Circuit Summary, Frequency Selection

The frequency selection is performed by the two printed circuit boards /211\ and /212\.

The purpose of this unit is to control the selection of the receiving frequency, display it and control the Synthesizer output frequency in accordance with this setting.

The frequency setting can be done in the following ways:

From the Keyboard any number (the receiving frequency) less than 30.000.0 can be keyed into the displays. This number can be changed in steps of 100 Hz by means of the Tuning Wheel provided that the LOCK-Key is not activated. If the LOCK-key is activated, the Tuning Wheel will be inoperative while the Keyboard will remain operative. When the Band switch is moved to the 500 kHz or 2182 kHz positions these frequency settings will override the present setting, which is saved and will appear again when the Band switch is moved to any other position

It is not possible to choose a number greater than 29.999.9; if such an attempt is made, the displays are automatically cleared and ready to accept a new frequency setting.

For any frequency setting less than 10.0 kHz the receiver is muted.

To display the frequency a multiplexing system is used. All the digit datas used to control the Synthesizer are present on a parallel form and in the code of BCD 9's complement right after the 500 kHz and 2182 kHz Preselection Circuits. In order to display the receiving frequency the Scan Counter selects via the Multiplexer unit, one of these digit data blocks at a time, converts it to BCD code and decodes it further to 7 segment information. This information controls a 7 segment Driver, which starts driving the appropriate digit-display, selected by the Scan Decoder. So, in fact, only one display is derived at a time but the repetition rate is so high that no flickering appears.

The Dimmer Control potentiometer is used to regulate the period of time in which the respective display is activated, thus controlling the light intensity of the displays. The light intensity of the meter is regulated simultaneously in the same manner.

The most significant digit is decoded to select the correct band of the VCO's of the Frequency Synthesizer.

5.8. Circuit Description, Frequency Selection.

5.8.1. /211\ Display and Keyboard

When a key (except for the LOCK-key) is depressed the associated key-number is partly encoded in IC1 and passed on to an additional encoder located on /212\ to complete the BCD 9's Complement encoding. Furthermore IC1 serves as an N-key lock-out unit, i.e. if one or more keys have already been depressed, it is not possible to activate the Keyboard before all depressed keys are released. If two or more keys are depressed simultaneously the lowest key-number is chosen.

The Tuning Control consists of a Tuning Wheel, two optically coupled modules, and an UP/DOWN-Control. The Tuning Wheel is a thin metal disk in which holes are etched. The two optically coupled modules sense these holes, and produce a pulse for each hole encountered. Each pulse counts up or down the displayed number, provided that the LOCK-key is not activated. The direction of this counting is controlled by IC10.

By means of the two potentiometers R26 and R27 it is possible to adjust the duty cycles of the output from the two Smith-triggers (IC9) to 50%. When the wheel is rotated the outputs will exhibit a phase difference of 90° if the optically coupled modules are correctly mounted. This is necessary to ensure proper functioning of the UP/DOWN-Control.

The heart of the multiplex system is the combined Clock Generator and Dimmer Control consisting of IC4 together with external components, of which the potentiometer regulates the duty cycle of the clock.

This Clock Generator drives the Scan Counter which again produces the Scan Address. This address decides which digit the multiplex system is to operate on. The Scan Decoder selects via a driver transistor, the appropriate digit l.e.d. display.

The multiplexed BCD-input from 212 after being decoded into the 7-segment code in IC15 decides which figure is to be shown in the display.

Two other signals from 212 control IC15. One signal derived from the multiplex clock, is fed to the RBo terminal. Due to the variable duty cycle of the multiplex clock, it is possible to control within a clock cycle the ratio between how long the outputs of IC15 are enabled and disabled, thus controlling the light intensity of the display. The other signal is a blanking control signal, which is led to the RBi terminal, completely blanking the displays that would otherwise show irrelevant zeros.

Because of the high peak currents driving the displays, the segment driving is performed by a special high current array, IC14.

The displays show the frequency in kHz and the decimal point is the only light source, which is not dimmable.

The AGC-voltage from board 205 is shown on the meter; the light intensity of the associated bulb is controlled by the Dimmer Control in the same way as the displays.

5.8.2. 212 Synthesizer Control

When a key is depressed or released there will always be some sort of bouncing effect before the key has settled. This bouncing is removed by means of the Key Bounce Eliminator consisting of IC4 and additional external gates. A load-command for the Digit Register Stack consisting of six programmable up/down-counters is generated as long as a key (except for the LOCK-key) is depressed. A clock pulse is produced when the key has settled after being activated, and the data corresponding to the key number is loaded into IC10 and simultaneously all the data present in the Digit Register Stack is shifted to the next counter.

The encoding of the key-number is completed on this board before entering the Digit Register Stack.

To clear this stack the last half of IC4 is triggered by means of the multiplex clock and, simultaneously data corresponding to key-number "0" is produced. So for each clock cycle these datas are read into the Data Register Stack.

When the Tuning Wheel is rotated a pulse is generated in the Pulse Shaper each time a hole passes the optically coupled modules on /211\ . This pulse activates the last half of the Key Bounce Eliminator which produces a counting pulse for the Digit Register Stack, thus incrementing or decremeting on /211\ . If the LOCK-key is activated, the counters IC10 and IC11 will become disabled thus making it impossible to tune the receiver in the way mentioned above, but the Keyboard will remain operative.

The outputs of the Data Register Stack are led through the 500 kHz and 2182 kHz Preselection circuits, IC16-IC21. If neither of these two Band-settings is chosen the data passes through these gates. Otherwise one of the two preselected frequency number is chosen independent of the content of the Digit Register Stack.

By means of IC29 it is tested every 8th cycle of the multiplex clock, whether the most significant digit is greater than 2 or not, if it is, then a Clear command identical to that produced by means of the Clear-key is generated through the subsequent 8th clock cycle.

The data now containing the information of the receiving frequency in BCD 9's complement is then used for two purposes. First to control the Frequency Synthesizer and second to feed the displays.

The four multiplexers select one digit data block, controlled by the Scan Address, and pass it on through a BCD 9's Complement Converter before it enters /211\ in order to become displayed there.

In order to establish a so-called leading edge zero suppression of the displayed frequency, the latch consisting of two gates from IC7 controls the blanking input of RB_1 of the BDC 7 segment decoder on /211\ . This latch is reset by clock pulse number six and seven whereby the blanking input is activated. Through the four inverters of IC31 the latch senses the first zero to come, beginning with the most significant digit. The first digit different from zero sets the latch, thus cancelling the blanking command. If all the digits are equal to zero, a puls from /211\ sets the latch on clock pulse number five, so that the least significant digit is always displayed.

In order to mute the receiver, if the receiving frequency setting is less than 10 kHz, the output from the latch mentioned above is sampled on the third clock pulse, this deciding whether the four most significant digits are all different from zero or not. If they all are equal to zero a mute command is produced.

The most significant digit is decoded in order to control the band selection of the VCO's of the Frequency Synthesizer.

5.9. Circuit Description, P 5013, 24VDC/AC Power Pack

5.9.1. (286) Transformers and Converter

A double pole mechanically operated safety switch is inserted in the AC mains input leads. The primary current of the mains transformer T1 is controlled by the front panel mounted POWER-switch.

The secondary windings of T1 are connected to two sets of rectifiers.

Input current from the battery input terminal is also controlled by the POWER-switch. An RFI-filter on board (287) is followed by Zener diode D1.

Diode D1 protects the converter against transients on the supply leads and against the consequences of polarity reversal of the battery supply leads. The converter is composed of transistors TR1 and TR2 and the square wave output signal is coupled through transformer T2 to two sets of rectifiers.

5.9.2. (287) Converter Driver, Rectifiers and Stabilizers

A bistable multivibrator composed of transistors TR1 and TR5 is driven from oscillator TR4 with the nominal frequency 400 Hz. The output signals from the multivibrator are therefore square waves with a repetition frequency of 200 Hz, and these signals having a phase difference of 180° are used as driving signals for the converter. One output signal from transformer 286T2 is fed to a double rectifier followed by a voltage stabilizer having a nominal voltage of 15.7V, while a second output signal after rectification also in a double rectifier is fed to a voltage stabilizer having a nominal output voltage of 7.5V.

A mains voltage sensor composed of transistors TR2, TR3 and TR6 controls, via RL2, the 24V converter and the 24V SUPPLY indicator.